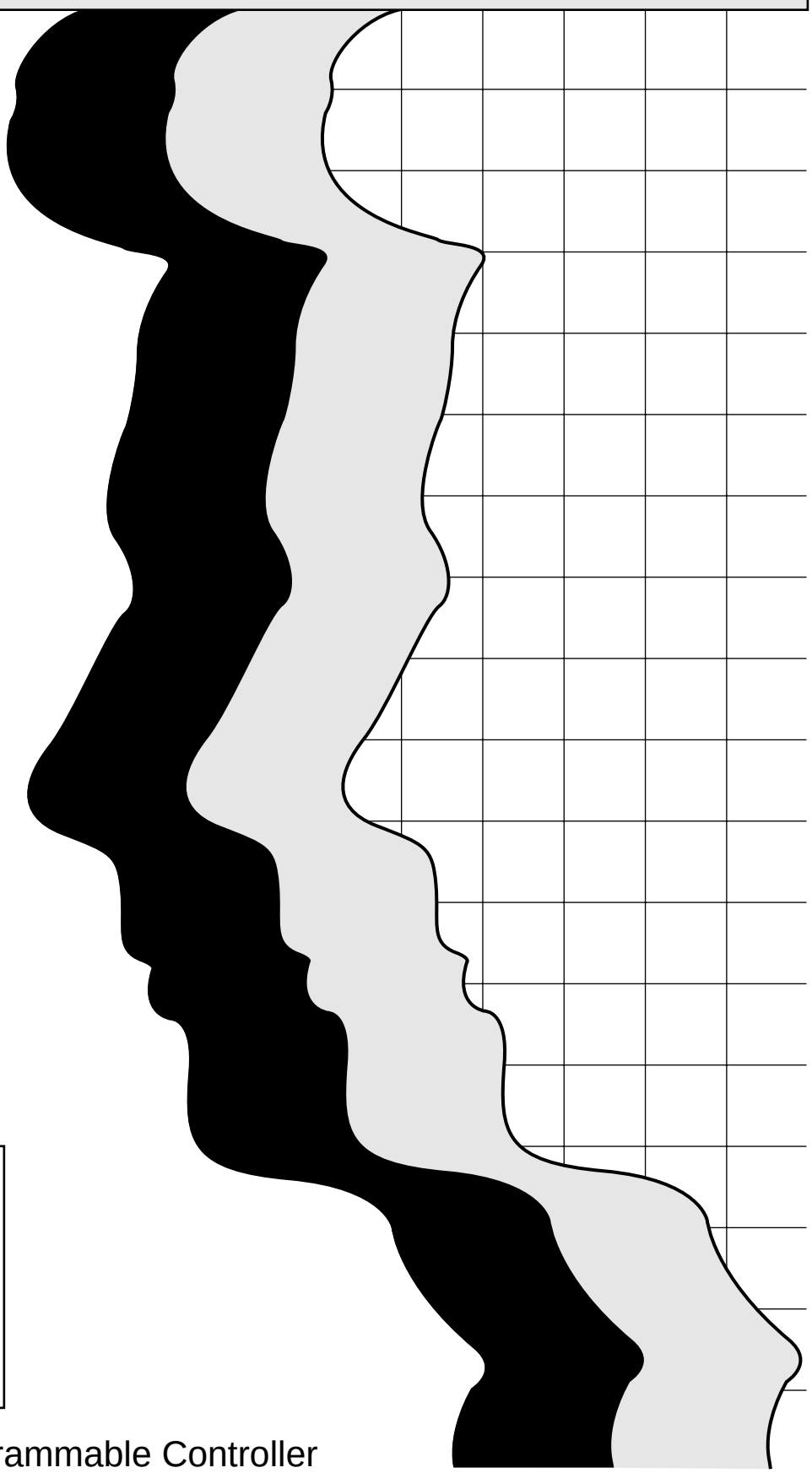
MITSUBISHI

Analog-Digital Converter Module type A68ADC

User's Manual



MELSEC

Mitsubishi Programmable Controller

● SAFETY PRECAUTIONS ●

(Read these precautions before using.)

When using Mitsubishi equipment, thoroughly read this manual and the associated manuals introduced in this manual.
Also pay careful attention to safety and handle the module properly. These precautions apply only to Mitsubishi equipment. Refer to the CPU module user's manual for a description of the PLC system safety precaution.
These ● SAFETY PRECAUTIONS ● classify the safety precautions into two categories: "DANGER" and "CAUTION".

⚠ DANGER	**Procedures which may lead to a dangerous condition and cause death or serious injury if not carried out properly.**
⚠ CAUTION	**Procedures which may lead to a dangerous condition and cause superficial to medium injury, or physical damage only, if not carried out properly.**

Depending on circumstances, procedures indicated by ⚠ **CAUTION** may also be linked to serious results.
In any case, it is important to follow the directions for usage.
Store this manual in a safe place so that you can take it out and read it whenever necessary. Always forward it to the end user.

[DESIGN PRECAUTIONS]

⚠ DANGER

- Install a safety circuit external to the PLC that keeps the entire system safe even when there are problems with the external power supply or the PC module. Otherwise, trouble could result from erroneous output or erroneous operation.
  (1) Outside the PLC, construct mechanical damage preventing interlock circuits such as emergency stop, protective circuits, positioning upper and lower limits switches and interlocking forward /reverse operations.
  (2) When the PLC detects the following problems, it will stop calculation and turn off all output.
    - The power supply module has over current protection equipment and over voltage protection equipment.
    - The PLC CPUs self-diagnostic functions, such as the watchdog timer error, detect problems. In addition, all output will be turned on when there are problems that the PLC CPU cannot detect, such as in the I/O controller. Build a fail safe circuit exterior to the PLC that will make sure the equipment operates safely at such times. See user's manual for example fail safe circukts.

    See this user's manual for example fail safe circukts.
  (3) Output could be left on or off when there is trouble in the outputs module relay or transistor. So build an external monitoring circuit that will monitor any single outputs that could cause serious trouble.
- When overcurrent which exceeds the rating or caused by short-circuited load flows in the output module for a long time, it may cause smoke or fire. To prevent this, configure an external safety circuit, such as fuse.
- Build a circuit that tums on the external power supply when the PLC main module power is turned on. If the external power supply is turned on first, it could result in erroneous output or erroneous operation.
- When there are communication problems with the data link, the communication problem station will enter the following condition.
  Build an interlock circuit into the PLC program that will make sure the system operates safely by using the communication state information. Not doing so could result in erroneous output or erroneoud operation.
  (1) For the data link data, the data prior to the communication error will be held.
  (2) The MELSECNET (II,/B,/10) remote I/O station will turn all output off.
  (3) The MELSECNET/MINI-S3 remote I/O station will hold the output or turn all output off depending on the E.C. remote setting.

  Refer to the data link manuals regarding the method for setting the communication problem station and the operation status when there are communication problem.
- When configuring a system, do not leave any slots vacant on the base. Should there be any vacant slots, always use a blank cover (A1SG60) or dummy module (A1SG62).
  When the extension base A1S52B, A1S55B or A1S58B is used, attach the dustproof cover supplied with the product to the module installed in slot 0.
  If the cover is not attached, the module's internal parts may be dispersed when a short-circuit test is performed or overdurrent/overvoltage is accidentally applied to the external I/O area.

⚠ CAUTION

- Do not bunch the control wires or communication cables with the main circuit or power wires, or install them close to each other. They should be installed 100 mm (3.94 inch) or more from each other. Not doing so could result in noise that would cause erroneous operation.

[DESIGN PRECAUTIONS]

⚠ CAUTION

- When controlling items like lamp load, heater or solenoid valve using an output module, large current (approximately ten times greater than that present in normal circumstances) may flow when the output is turned OFF→ON. Take measures such as replacing the module with one havingsufficient rated current.

[INSTALLATION PRECAUTIONS]

⚠ DANGER

- Use the PLC in an environment that meets the general specifications contained in this manual. Using this PLC in an environment outside the range of the general specifications could result in electric shock, fire, erroneous operation, and damage to or deterioration of the product.
- Install so that the pegw on the bottom of the module fit securely into the base unit peg holes, and use the specified torque to tighten the module's fixing screws. Not installing the module correctly could reault in erroneous operation, damage, or pieces of the product falling.
- Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.
- When installing more cables, be sure that the base unit and the module connectors are installed correctly. After installation, check them for looseness. Poor connections could result in erroneous input and erroneous output.
- Correctly connect the memory cassette installation connector to the memory cassette. After installation, be sure that the connection is not loose. A poor connection could result in erroneous operation.
- Do not directly touch the module's conductive parts or electronic components. Doing so could cause erroneous operation or damage of the module.

[WIRING PRECAUTIONS]

⚠ DANGER

- Completely turn off the external power supply when installing or placing wiring. Not completely turning off all power could result in electric shock or damage to the product.
- When turning on the power supply or operating the module after installation or wiring work, be sure that the module's terminal covers are correctly attached. Not attaching the terminal cover could result in electric shockl.

⚠ CAUTION

- Be sure to ground the FG terminals and LG terminals to the protective ground conductor. Not doing so could result in electric shock or erroneous operation.
- When wiring in the PLC, be sure that it is done correctly by checking the product's rated voltage and the terminal layout. Connecting a power supply that is different from the rating or incorrectly wiring the product could result in fire or damage.

[WIRING PRECAUTIONS]

⚠CAUTION

- Do not connect multiple power supply modules in parallel. Doing so could cause overheating, fire or damage to the power supply module. If the terminal screws are too tight, it may couse falling, short circuit or erroneous operation due to damage of the screws or module.
- Tighten the terminal screws with the specified torque. If the terminal screws are loose, it could result in short circuits, fire, or erroneous operation.
- Tightening the terminal screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.
- Be sure there are no foreign substances such as sawdust or wiring debris inside the module. Such debris could cause fires, damage, or erroneous operation.
- External connections shall be crimped or pressure welded with the specified tools, or correctly soldered. For information regarding the crimping and pressure welding tools, see the I/O module's user's manual. Imperfect connections could result in short circuit, fires, or erroneous operation.

[STARTUP AND MAINTENANCE PRECAUTIONS]

⚠DANGER

- Do not touch the terminals while power is no. Doing so could cause shock or erroneous operation.
- Correctly connect the battery. Also, do not charge, disassemble, heat, place in fire, short circuit, or solder the battery. Mishandling of battery can cause overheating or cracks which could result in injury and fires.
- Switch all phases of the external power supply off when cleaning the module or tightening the terminal screws. Not doing so could result in electric shock. If the screws are too tight, it may cause falling, short circuit or erroneous operation due to damage of the screws or modules.
- Tightening the screws too far may cause damages to the screws and/or the module, resulting in fallout, short circuits, or malfunction.

⚠CAUTION

- The online operations conducted for the CPU module being operated, connecting the peripheral device (especially, when changing data or operation status), shall be conducted after the manual has been carefully read and a sufficient check of safety has been conducted. Operation mistakes could cause damage or trouble of the module.
- Do not disassemble or modify the modules. Doing so could cause trouble, erroneous operation, injury, or fire.
- Switch all phases of the external power supply off beforw mounting or removing the module. If you do not switch off the external power supply, it will cause failure or malfunction of the module.
- Always use the designated fuse for replacement.
  Using a larger capacity fuse or wire could cause a fire.

[DISPOSAL PRECAUTIONS]

⚠CAUTION

- When disposing of this product, treat it as industrial waste.

REVISIONS

※The manual number is given on the bottom left of the back cover.

Print Date	※Manual Number	Revision
May, 1990	IB (NA) 66247-A	First edition
Apr., 2001	IB (NA) 66247-B	Addition Appendix 1, 2, 3, WARRANTY Correction SAFETY PRECAUTIONS, Chapter 1, Section 2.1, 2.2.1, 2.2.2, 3.1.2, 3.2.2, 3.3, 3.5.1, 3.5.4, 3.5.5, 3.6, 4.1.3, 4.2.2, 4.6.3, 4.6.4, 4.7, 5.1.1, 5.1.3, 5.2.1, 5.2.2, 5.3.2, 5.4.1, 5.4.2, 5.6.1, 5.6.3, 5.6.4, 5.7, 6.2, 6.3, 6.4, 6.7.1, 6.7.2, 6.8.2, 6.9.2, 7.1, 7.4, Appendix 4.5

INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

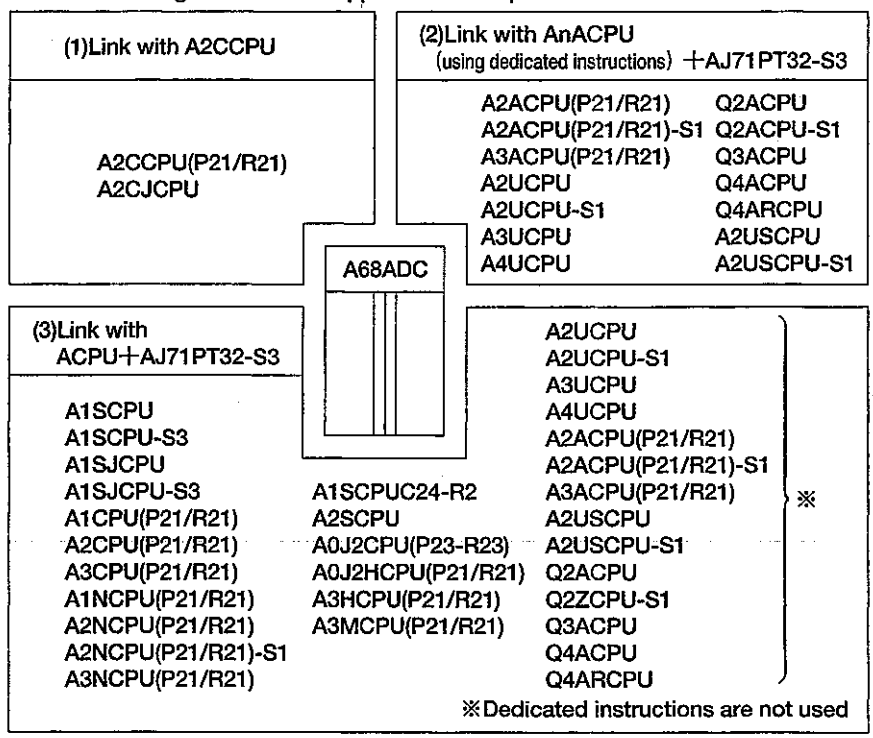
1. INTRODUCTION

This User's Manual describes the specifications, handling and programming procedures of the A68ADC analog-digital converter module (hereinafter called "the A68ADC") to be used in combination with the A2CCPU or as a remote station in the MELSECNET/MINI-S3 data link system.

The A68ADC is used to convert incoming analog signals (voltage or current inputs) to 16-bit signed BIN (11-bit data part) digital data.
Please refer to the following manuals if necessary for the use of the A68ADC.

ACPU Programming Manual (Fundamentals) IB(NA)66249
ACPU Programming Manual (Common Instructions) IB(NA)66250
A2A(S1)/A3ACPU Programming Manual (Dedicated Instructions) IB(NA)66251
A2CCPU User's Manual IB(NA)66238
AJ71PT32-S3 MELSECNET/MINI-S3 Master Unit User's Manual IB(NA)66217
SW0GP-MINIP Operating Manual IB(NA)66226

The following are the CPUs applicable to the paths for link with the A68ADC.



1.1 Features

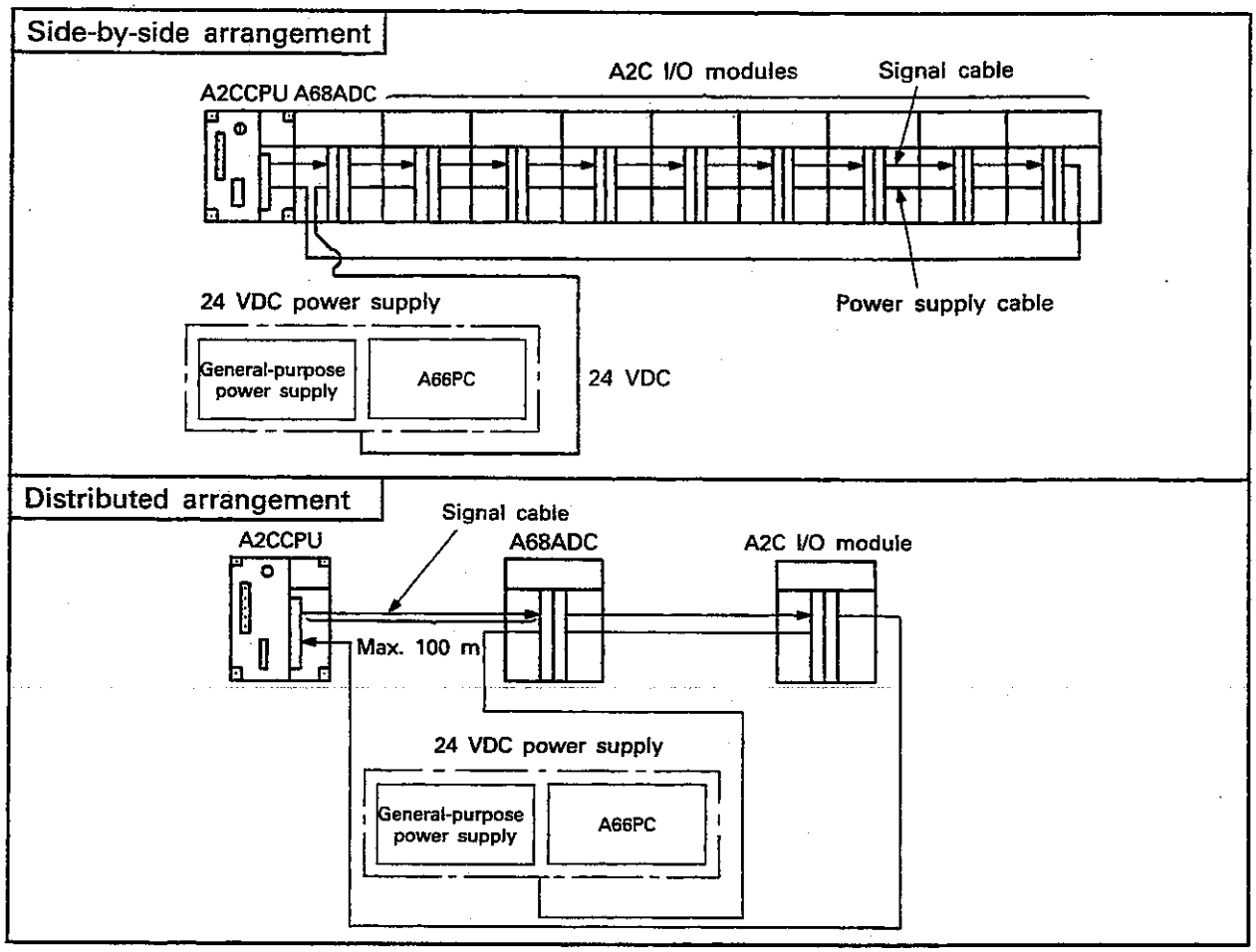
(1) Allows connection to external sensors up to 8 channels.

(2) Three different processings of time averaging, count averaging and sampling are usable for analog-digital (A/D) conversion.

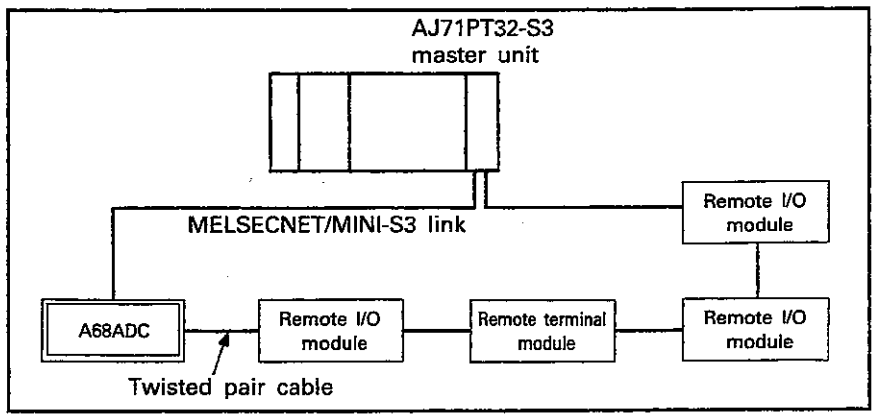
(3) A/D conversion enable/disable can be set independently for each channel.

(4) The A/D conversion speed per channel is 2.5 ms.

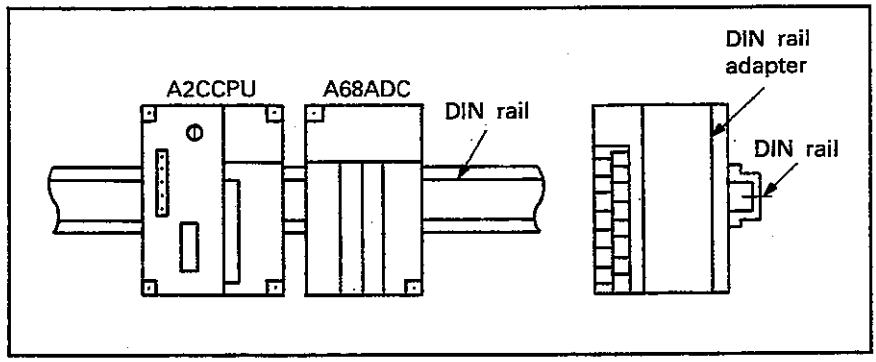
(5) Connects to the A2CCPU by flat cables, twisted pair cables or shielded PVC cables. Installation can be arranged as side-by-side or as distributed. The maximum length of cables connecting between the A68ADC and the A2CCPU in distributed arrangement is 100 m.



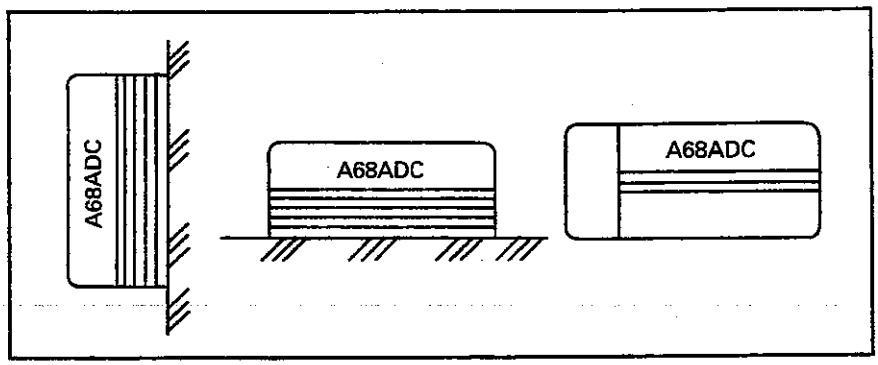
(6) Usable as a remote terminal module of the MELSECNET/MINI-S3 link.



(7) Can be mounted to the DIN rail using the DIN rail adapter.



(8) Designed compact: 170 mm high × 100 mm wide × 80 mm long. Can be mounted in a small space and in any position.



2. GENERAL SPECIFICATIONS

2.1 General Specifications

Table 2.1 shows the common specifications of various modules used.

<table>
<tr><th>Item</th><th colspan="6">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="6">0 to 55℃</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="6">-20 to 75℃</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="6">10 to 90%RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="6">10 to 90%RH, non-condensing</td></tr>
<tr><td rowspan="5">Vibration resistance</td><td rowspan="5">Conforming to JIS* B 3501, IEC 61131-2</td><td>———</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>No. of sweeps</td></tr>
<tr><td rowspan="2">under intermitten vibration</td><td>10 to 57 Hz</td><td>———</td><td>0.075 mm (0.003 in.)</td><td rowspan="4">10 times each in X, Y, Z directions (for 80 min.)</td></tr>
<tr><td>57 to 150 Hz</td><td>9.8m/S²</td><td>———</td></tr>
<tr><td rowspan="2">under continuous vibration</td><td>10 to 57 Hz</td><td>———</td><td>0.035 mm (0.001 in.)</td></tr>
<tr><td>57 to 150 Hz</td><td>4.9m/S²</td><td>———</td></tr>
<tr><td>Shock resistance</td><td colspan="6">Conforming to JIS B3501, IEC 61132-2 (147m/S², 3 times in each 3 directions X Y Z)</td></tr>
<tr><td>Operating ambience</td><td colspan="6">No corrosive gases</td></tr>
<tr><td>Operating elevation</td><td colspan="6">2000 m (6562 it.) max.</td></tr>
<tr><td>Installation location</td><td colspan="6">Control panel</td></tr>
<tr><td>Over-voltage categry *1</td><td colspan="6">II max.</td></tr>
<tr><td>Pollution level *2</td><td colspan="6">2 max.</td></tr>
</table>

Table 2.1 General Specifications

*1: This indicates the section of the power supply to which the equipmen is assumed to be connected between the public electrical power distribution network and the machinery within the premises. Category II applies to equipment for which electrical power is supplied from fixed facilities. The surge voltage withstand level for up to the rated voltage of 300V is 2500V.

*2: This index indicates the degree to which conductive material is generated in terms of the environment in which the equipment is used. Pollution level 2 is when only non-conductive pollution occurs. A temporary conductivity caused by condensation must be expected occasionally.

Note: * JIS: Japanese Industrial Standard

2.2 Performance Specifications

2.2.1 Specifications

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Analog input</td><td>Selection depends on input terminals.
Voltage: −10 to 0 to +10 VDC (input resistance: 30 KΩ)
Current: +4 to +20 mADC (input resistance: 250 Ω)
*−20 to 0 +20 mA can also be used for current input.</td></tr>
<tr><td>Digital output</td><td>16-bit, signed binary (11-bit data part) −2048 to +2047</td></tr>
<tr><td>I/O characteristics</td><td><table><tr><th>Analog Input</th><th>Digital Output</th></tr><tr><td>+10 V</td><td>+2000</td></tr><tr><td>+5 V or +20 mA</td><td>+1000</td></tr><tr><td>0 V or +4 mA</td><td>±0</td></tr><tr><td>−5 V or −12 mA</td><td>−1000</td></tr><tr><td>−10 V</td><td>−2000</td></tr></table>*See Section 2.2.2 for details.</td></tr>
<tr><td>Maximum resolution</td><td>*1 Voltage: 5 mV (1/2000)
Current: 20 μA (1/1000)</td></tr>
<tr><td>Overall accuracy
(Accuracy with respect to the maximum value)</td><td>*1 Within ±1% (±20)</td></tr>
<tr><td>Maximum conversion speed</td><td>*2 Maximum 2.5 ms/channel</td></tr>
<tr><td>Absolute maximum input</td><td>Voltage: ±15 V
Current: ±30 mA</td></tr>
<tr><td>Number of analog input points</td><td>8 channels/unit</td></tr>
<tr><td>Insulation method</td><td>Photocoupler insulation between output terminals and PLC power
(Non-insulated between channels)</td></tr>
<tr><td>Occupied I/O stations (points)</td><td>4 stations (32 points)</td></tr>
<tr><td>Connection terminal</td><td>47-point terminal block</td></tr>
<tr><td>Applicable wire size</td><td>0.75 to 2 mm^2 (18 to 14 AWG)(Applicable tightening torque: 39~59 N-cm)</td></tr>
<tr><td>Applicable solderless terminal</td><td>V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A</td></tr>
<tr><td>24 VDC internal current consumption</td><td>0.3</td></tr>
<tr><td>Weight kg (lb)</td><td>1.01 (2.22)</td></tr>
<tr><td>Outside dimensions mm (in)</td><td>170 (6.69) (H) × 100 (3.94) (W) × 80 (3.15) (D)</td></tr>
</table>

Table 3.2 Performance Specifications

POINT

***1 Analog input allowed for maximum resolution and overall accuracy, is from −10 to 0 to +10 V or from −20 to 0 to +20 mA.**

***2 The maximum conversion speed indicates that of a single A68ADC module. The time required for the PC CPU to read digital output after A/D conversion should be the maximum conversion speed plus the time required for communication with the A68 ADC. For details of the communication processings, see Sections 3 and after describing processing time for types of CPUs.**

2.2.2 I/O conversion characteristics

I/O conversion characteristics are dictated by the offset value and gain value set in test mode. Fig. 2.1 shows an example for voltage input.

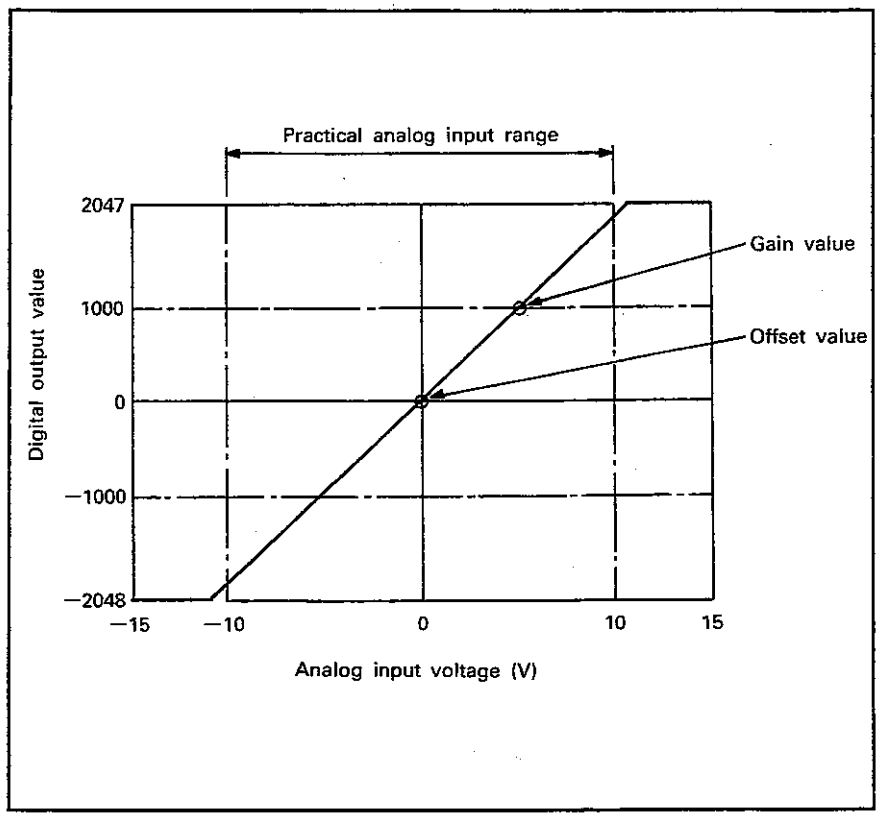


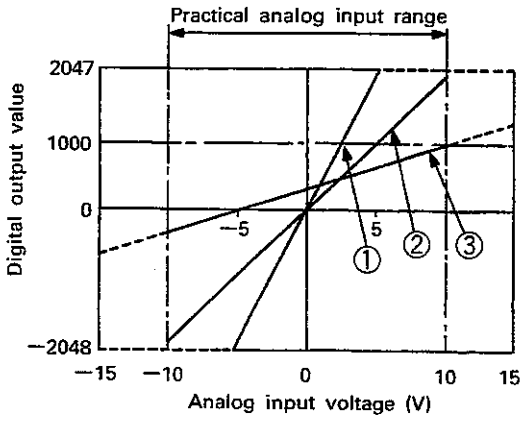
Fig. 2.1 I/O Conversion Characteristics

REMARK

(1) The offset value is the analog input (voltage or current) value at which the digital output value is 0. Set the offset value in test mode.
(2) The gain value is the analog input (voltage or current) value at which the digital output value is 1000. Set the gain value in test mode.

(1) Voltage input characteristic

Fig. 2.2 shows the voltage characteristics for three different offset/gain combinations.



The offset/gain setting in the figure at left is as follows.

(1) When the offset value is 0 V and the gain value is 2.5 V, the characteristic is as indicated by ①.
Example:
When the analog input value is 3 V, the digital output value is 1200.
When the analog input value is −3 V, the digital output is −1200.

(2) When the offset value is 0 V and the gain value is 5 V, the characteristic is as indicated by ②.
Example:
When the analog input value is 3 V, the digital output value is 600.
When the analog input value is −3 V, the digital output value is −600.

(3) When the offset value is −5 V and the gain value is 10 V, the characteristic is as indicated by ③.
Example:
When the analog input value is 3 V, the digital output value is 533.
When the analog input value is −3 V, the digital output value is 133.

Fig. 2.2 Voltage Input Characteristic

POINT

(1) When the input voltage is in the range from −10 to 0 to +10 V, the maximum resolution and overall accuracy are within the quoted range of performance specifications. However, if this range is exceeded, resolution and accuracy will be impaired.

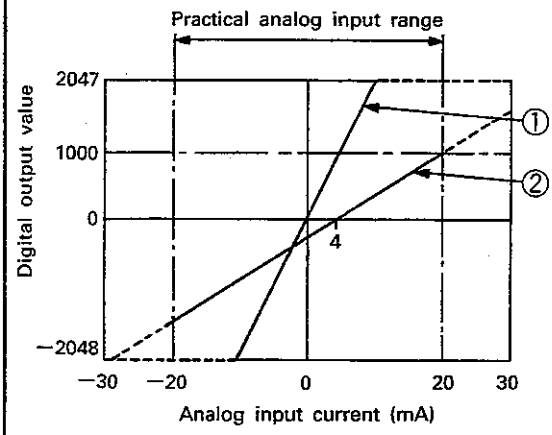
(2) If an analog input corresponding to a digital output value of more than +2047 or −2048 is applied, the digital output value will not exceed +2047 or −2048.

(3) Do not apply ±15 V or more. this will damage the unit.

(4) In offset/gain setting, the offset value should always be less than the gain value. If the offset value is greater than or equal to the gain value, the digital output value will be unpredictable.

(2) Current input characteristic

Fig. 2.3 shows the current characteristics for two different offset/gain combinations.



The offset/gain setting in the figure at left is as follows.

(1) When the offset value is 0 mA and the gain value is 5 mA, the characteristic is as indicated by ①.
Example:
When the analog input value is 7 mA, the digital output value is 1400.
When the analog input value is −3 mA, the digital output value is −600.

(2) When the offset value is 4 mA and gain value is 20 mA, the characteristic is as indicated by ②.
Example:
When the analog input value is 7 mA, the digital output value is 187.
When the analog input value is −3 mA, the digital output value is −437.

Fig. 2.3 Current Input Characteristic

POINT

(1) When the input current is in the range from −20 to 0 to +20 mA, the maximum resolution and overall accuracy are within the quoted range of performance specifications. However, if this range is exceeded, resolution and accuracy will be impaired.

(2) If an analog input, corresponding to a digital output value of more than +2047 or −2048 is applied, the digital output value will not exceed +2047 or −2048.

(3) Do not apply ±30 mA or more. This will damage the unit.

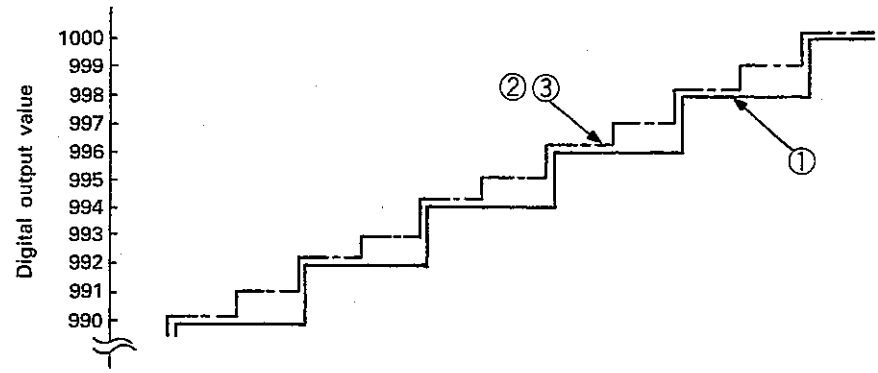
(4) In offset/gain setting, the offset value should always be less than the gain value. If the offset value is greater than or equal to the gain value, the digital output value will be unpredictable.

(3) Relation between offset/gain setting and digital output value

The maximum resolution of the A68ADC is 5 mV in voltage and 20 μA in current. Maximum resolution may be found using the following expression:

$$\frac{\text{(Gain value)} - \text{(offset value)}}{1000} < \text{(maximum resolution)}$$

Fig. 2.4 and 2.5 show the relation between the offset/gain setting and the digital output value for the offset/gain settings in Fig. 2.2 and 2.3.

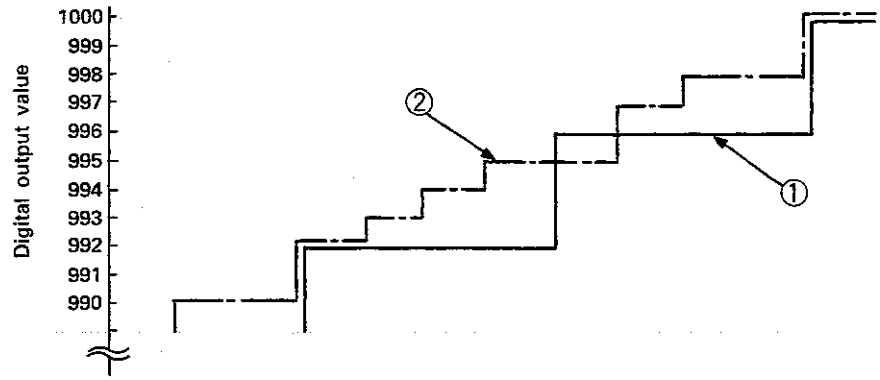


NO	Offset	Gain											
①	0	2.5	—	2.475 to 2.480	2.480 to 2.485	2.485 to 2.490	2.490 to 2.495	2.495 to 2.500	2.500 to 2.505				
②	0	5	—	4.950 to 4.955	4.955 to 4.960	4.960 to 4.965	4.965 to 4.970	4.970 to 4.975	4.975 to 4.980	4.980 to 4.985	4.985 to 4.990	4.990 to 4.995	4.995 to 5.000	5.000 to 5.005
③	−5	10	—	9.850 to 9.865	9.865 to 9.880	9.880 to 9.895	9.895 to 9.910	9.910 to 9.925	9.925 to 9.940	9.940 to 9.955	9.955 to 9.970	9.970 to 9.985	9.985 to 10.000	10.000 to 10.015

□ or more at top to Less than □ at bottom

*: For ①, (gain value − offset value)/1000 < 5 mV, so the digital value does not increase or decrease in units of one count.

Fig. 2.4 Voltage Input and Digital Output Value



NO	Offset	Gain											
①	0	5	—	4.96 to 4.98				4.98 to 5.00				5.00 to 5.02	
②	4	20	—	19.84 to 19.86	19.86 to 19.88	19.88 to 19.90	19.90 to 19.92	19.92 to 19.94	19.94 to 19.96	19.96 to 20.00			20.00 to 20.02

□ or more at top to Less than □ at bottom

*: For ① and ②, since (gain value − offset value)/1000 < 20 μA, the digital value does not always increase or decrease in units of one count.

Fig. 2.5 Current Input and Digital Output Value

(4) Overall precision

Overall precision is the precision of the maximum value of the digital output value.
Even if the offset and gain settings are changed and the input characteristics are changed, the overall precision does not change and remains within the range shown in the specifications. Overall precision for the power supply and current input characteristics are shown in Fig. 2.6 and Fig. 2.7.

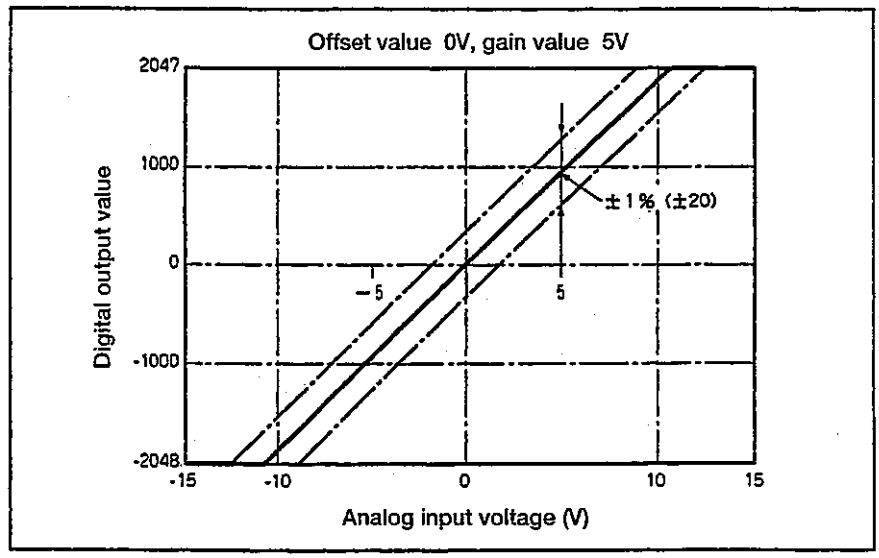


Fig. 2.6 Overall precision for voltage input characteristics

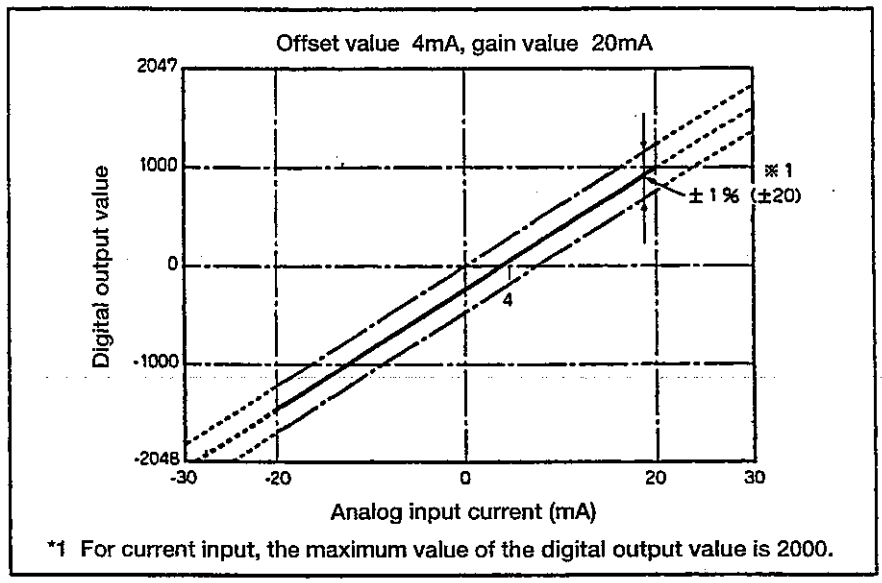


Fig. 2.7 Overall precision for current input characteristics

2.3 Sampling Processing A/D Conversion System

The analog values input to the channels designated for sampling processing by the PLC CPU are converted to digital output values one by one and the digital output values are stored in the buffer memory.

POINT

When sampling processing is designated:
As the A68ADC's CPU scans each channel, the value appearing at that instant is written to the buffer memory as a digital value. The timing of this sampling depends on the number of channels used, and may be found from the following expression.

(Processing time)

= (Number of channels used) × 2.5 (ms/channel)

↑

Max. conversion speed

(Example) When the number of channels is 5:

Processing time = 5 × 2.5 = 12.5 (ms)

2.4 Averaging Processing A/D Conversion System

The A68ADC makes the A/D conversion for any channels to which averaging processing has been specified from the PC CPU. Using a preset count or a preset period of time, an average is calculated (excluding the maximum value and the minimum value) and stored to the buffer memory. If the specified processing count is two or less, sampling processing is executed instead of averaging processing.
Setting ranges for count and time are as shown below.

Processing by count: ····· 1 to 4000 times
Processing by time: ····· 20 to 10000 ms

POINT

(1) Averaging processing by specifying time

(a) Unit of setting time is 10 ms. Values less than 10 ms are rounded down.
(Example) If 1234 ms is set, it is processed as 1230 ms.

(b) The number of times of processing of set time varies with the number of channels used for A/D conversion.
Processing count

$$= \frac{\text{Time setting}}{\text{Number of channels} \times 2.5\ (\text{ms/channel})}$$

Max. conversion speed

(Example) Number of channels = 4, Time setting = 1000 ms
1000 ÷ (4 × 2.5) = 100 times

(2) Averaging processing by specifying a number of counts
The time in which the average value by this processing is stored in the buffer memory varies with the number of channels used.
Processing time = Count setting × Number of channels × 2.5 (ms/channel)

Max. conversion speed

(Example) Number of channels = 4, Count setting = 500
500 × 4 × 2.5 = 5000 (ms)

2.5 Channel Designation

The A68ADC has 8 channels for A/D conversion each of which can be designated for execution or non-execution of A/D conversion. Using the PC CPU, channels on which A/D conversion is executed are designated with address 0 (channel designation) in the buffer memory. (Default is set for execution of A/D conversion on all channels.)

(Examples)

(1) Conversion speed when A/D conversion is set on all channels (default)

8 (channels) × 2.5 ms (conversion speed/channel)
= 20 ms

(2) Conversion speed when A/D conversion is set on channels 1 and 3.

2 (channels) × 2.5 ms (conversion speed/channel)
= 5 ms

The following processings are executed when channel designation data is written to the buffer memory at address 0 (channel designation address) using the PC CPU.

(1) Initializing for averaging processing
Data in the work area stored by the system of the A68ADC is cleared. Digital values stored in the buffer memory remains as the data before channel designation data is written. For example, if a new channel designation data is written when sampling has been executed 30 times on a channel for which averaging processing is set for 50 times, the sampling data of 30 times is cleared and averaging processing starts from the initial status.

(2) Reset of the A/D conversion completion flag
The A/D conversion completion flag (buffer memory address 19) for channels 1 to 8 is reset.

2.6 Cautions on Using More Than One Channel

The A68ADC is provided with photocoupler insulation between the input terminals and the PC power supply. Channels are not insulated between each other.
Follow the instructions below if more than one channel is to be used on one module.

(1) Since the COM terminals for analog input are connected to each other in the module, make the voltage or current level equal on all COM terminals.

(2) If the voltage or current level is not equal on all COM terminals, use another A68ADC or provide insulation between channels outside the A68ADC.

2.7 Cable Specifications

Cables which can be used with the A68ADC are as follows.

(1) 5-core flat cable cut wiresThese cables, used when the A68ADC is installed adjacently to the A2CCPU or A2CCPU I/O module, can transmit data while supplying 24 VDC. Cable specifications are given below.

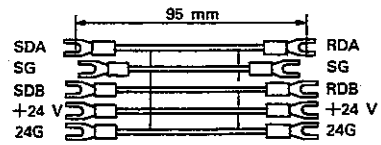
Model	A2C-005
Module intervals	0 ~ 34 mm
Conductor resistance	0.2 Ω
Insulation resistance (20 ℃)	15 MΩkm or larger
Dielectric withstand voltage V-min	200 VAC
Configuration	

Table 2.3 5-core Flat Cable Specifications1

(2) Twisted pair cable

Item	Specifications
Cable type	Shielded twisted pair cable
Logarithm	2P or larger
Conductor resistance (20 ℃)	88.0 Ω/km or less
Electrostatic capacity (1 kHz)	Average 60 nF/km or less
Characteristic impedance (100 kHz)	110 ± 10 Ω

Table 2.4 Twisted pair Cable Specifications

MEMO

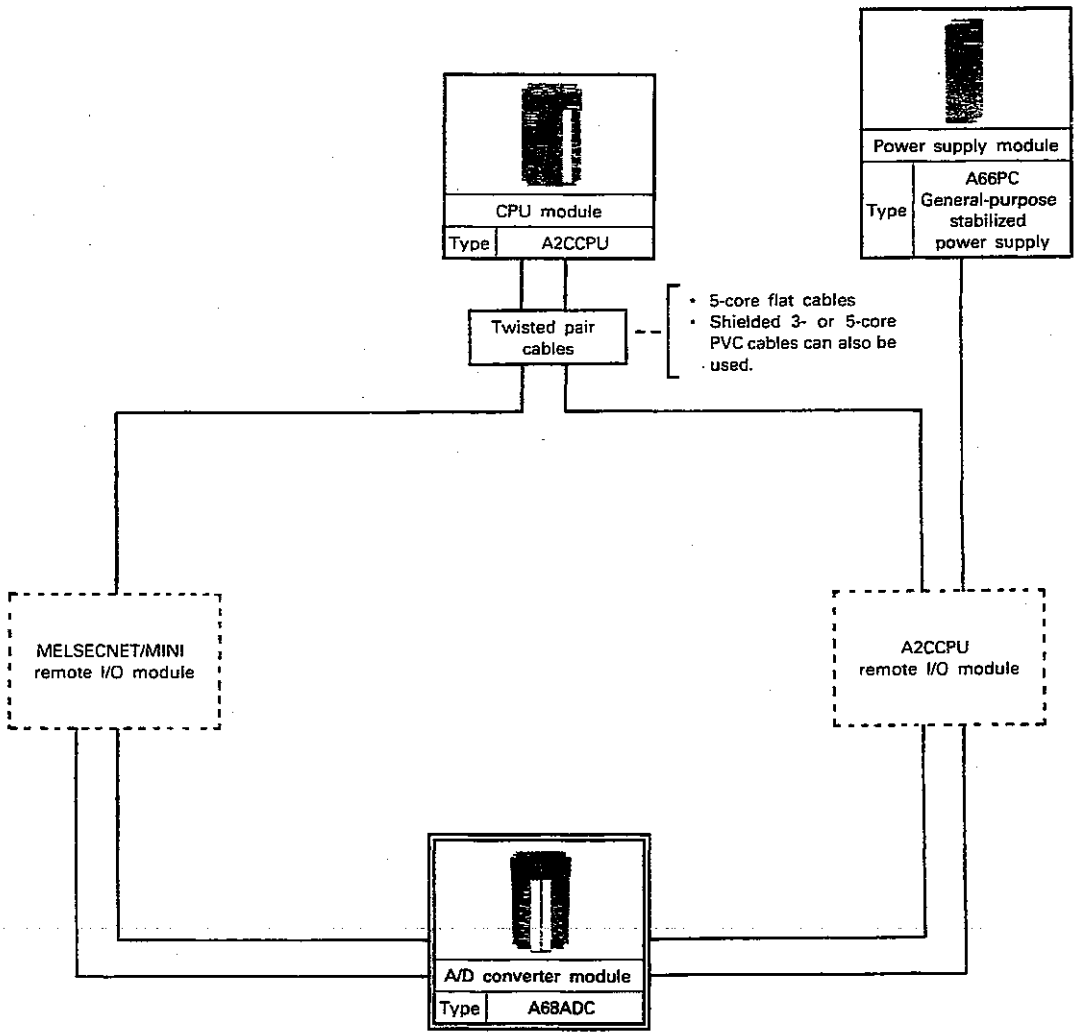
3. LINKING TO THE A2CCPU

The following sections describe the procedures to link the A68ADC to the A2CCPU. Booting systems SW4GP-GPPA, SW1S-GPPA or of previous type are equally applicable.

3.1 System Configuration

The following diagram shows when the A68ADC is used as a remote module of the A2CCPU.

3.1.1 Overall configuration



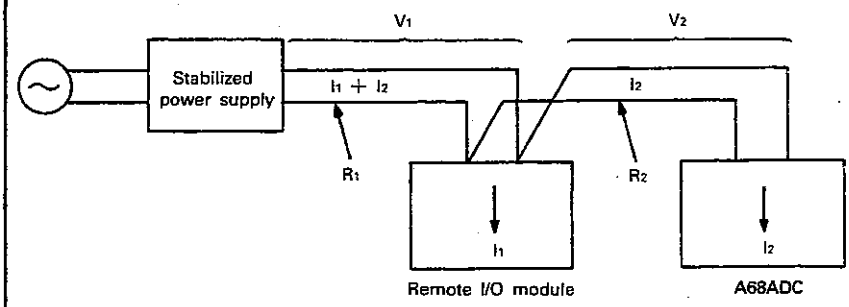
3.1.2 Cautions on constructing the system

(1) Flat cables, twisted pair cables and shielded 3- or 5-core PVC cables are used for connection between the A2CCPU and the A68ADC.
The maximum connecting distance between stations varies with cable size when twisted pair cables are used.

0.2 mm^2 to 0.5 mm^2 ····· 50 m
0.5 mm^2 and larger ····· 100 m

(2) The A68ADC requires external supply of 24 VDC power for internal power supply. Use the A66PC power supply module or a general-purpose stabilized power supply (24 VDC).

(3) When supplying power from one power supply to multiple A68ADCs or to the remote I/O modules, select proper cables and wiring route taking voltage drop into consideration.



V_1: Voltage drop between stabilized power supply and remote I/O module
V_2: Voltage drop between remote I/O module and A68ADC
R_1: Resistance between stabilized power supply and remote I/O module
R_2: Resistance between remote I/O module and A68ADC
I_1: Remote I/O module current consumption
I_2: A68ADC current consumption

Calculation of voltage drop

$V_1 = R_1 \times (I_1 + I_2)$
$V_2 = R_2 \times I_2$

Receiving port voltage of remote I/O module

(Receiving port voltage of remote I/O module)
= (Voltage of stabilized power supply) − V_1

(A68ADC receiving port voltage)
= (Voltage of stabilized power supply) − V_1 − V_2

Connection is possible if the receiving port voltage of A68ADC is within the range 15.6 V through 31.2 V.

3.2 Data Communication Processings

3.2.1 Communication method

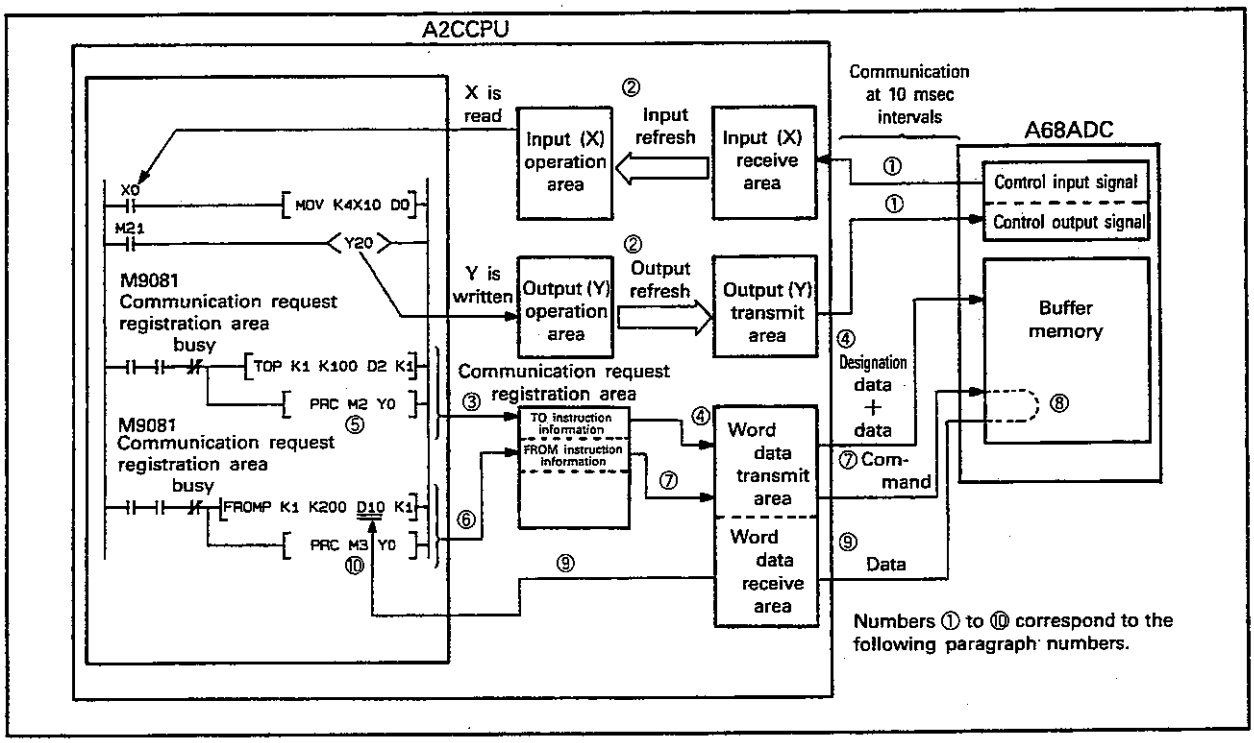


Fig. 3.1 Communication Processes

(1) Communication processes of control input/output signals used for interlocking of the A68ADC and the A2CCPU are described below. (See Section 3.3 for details of signals.)

① During sequence program execution, communication of input/output signals between the A2CCPU and the A68ADC is executed by suspending sequence program execution every 10 msec. During the communication, input signal data is stored in the input (X) receive area, and data stored in the output (Y) transmit area is output to the A68ADC.

② After the END instruction execution of the sequence program, data in the output (Y) operation area where operation result is stored is refreshed to the output (Y) transmit area, and then, data stored in the input (X) receive area is refreshed to the input (X) operation area.

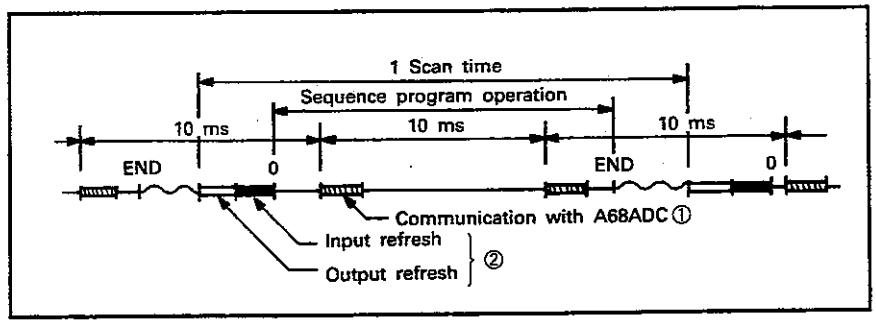


Fig. 3.2 Communication Timing of Input/output Signals

(2) Writing data to the A68ADC buffer memory

③ The TO instruction information is written to the communication request register area by the execution of the TO instruction, and registration of the TO instruction information is completed by execution of the PRC instruction.

④ By the execution of the PRC instruction, the TO instruction information stored in the communication request register area is transmitted in a few times of sending to the A68ADC via the word data transmit area after execution of the END instruction.
When the transmission has started, the PLC CPU starts processing the following steps. (The PLC CPU does not wait for the response of transmission completion before starting processing the following steps.)

⑤ The communication completion flag (device M2 in Fig. 3.1) designated by the PRC instruction is turned ON for 1 scan from step 0 of the scan immediately after the response of communication completion sent from the A68ADC is received by the A2CCPU. Upon communication completion, the TO instruction information stored in the communication request register area is cleared.

(3) Reading data from the A68ADC buffer memory

⑥ The FROM instruction information is written to the communication request register area by the execution of the TO instruction, and registration of the FROM instruction information is completed by execution of the PRC instruction.

⑦ By the execution of the PRC instruction, the FROM instruction information stored in the communication request register area is transmitted in a few times of sending to the A68ADC via the word data transmit area after execution of the END instruction.
When the transmission has started, the PLC CPU starts processing the following steps. (The PLC CPU does not wait for the response of transmission completion before starting processing the following steps.)

⑧ Upon receiving the FROM instruction information, the A68ADC sends data stored in the buffer memory of designated address back to the A2CCPU according to the information.

⑨ The read data is received by 1 word at 1 time of communication with the A68ADC and stored in the storage devices starting with that designated by the FROM instruction for the number of words designated.

⑩ The communication completion flag (device M3 in Fig. 3.1) designated by the PRC instruction is turned ON for 1 scan from step 0 of the scan immediately after the completion of storage of read data in designated devices.

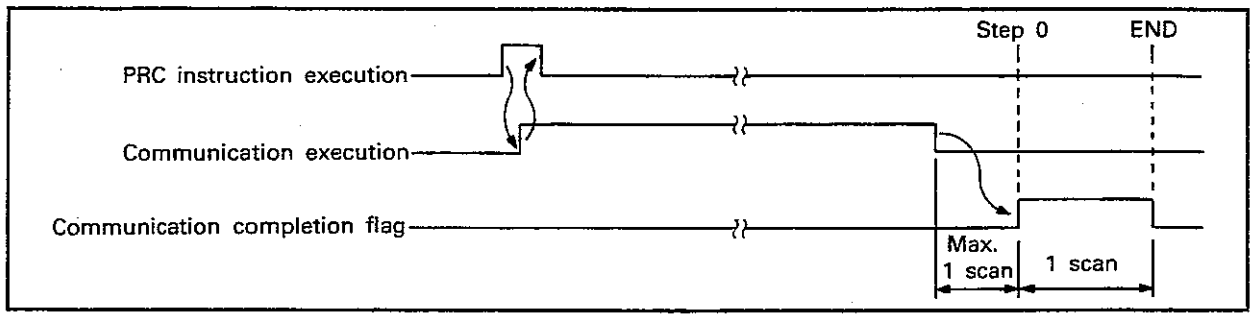


Fig. 3.3 Processing Timing of Data Reading and Writing

3.2.2 Processing time

This section introduces the processing time up to the writing of the A68ADC buffer memory data and processing time up to the reading of the data from the buffer memory.

(1) Processing time when writing data.

Maximum processing time
= 3 scan time *1 + 10ms × (number of write data words + 8) + 40ms *2

(2) Processing time when reading data

Maximum processing time
= 3 scan time *1 + 10ms × (number of read data words + 9) + 40ms *2

*1: The usage time for dedicated commands or partial refresh is 3 --> 1.
*2: A68ADC internal processing time.

3.3 Input/output Signals Handled With the A2CCPU

Functions of the control input and output signals handled between the A68ADC and A2CCPU are described in this section. Devices X refer to the input signals from the A68ADC to the A2CCPU. Devices Y refer to the output signals from the A2CCPU to the A68ADC. The actual device numbers for X/Y(n+0) to (n+1F) will differ from the setting number for the A68ADC as shown on page 3-10.

Signal direction: A68ADC → A2CCPU		Signal direction: A2CCPU → A68ADC	
Device No.	**Description**	**Device No.**	**Description**
X(n+0) to X(n+3)	Unusable	Y(n+0) to Y(n+3)	Unusable
X(n+4)	The communication error detection flag which is set if a communication error occurs by execution of the FROM/TO instructions.	Y(n+4)	Communication error reset signal *1
X(n+5)	Reset switch ON detection flag of the A68ADC module	Y(n+5)	Reset switch ON detection flag reset signal
X(n+6)	Unusable	Y(n+6)	Unusable
X(n+7)	Communication completion response signal wait flag	Y(n+7)	Retransmission request signl *1
X(n+8) to X(n+17)	Unusable	Y(n+8) to Y(n+1F)	Unusable
X(n+18)	A/D conversion ready (1) Turns ON when A/D conversion is ready in the normal mode (other than the test mode) after the power was turned on or the PLC CPU was reset. Turns OFF when mode is switched from normal to test. (2) Used for the interlock for reading and writing from the PLC CPU to the A68ADC.		
X(n+19) to X(n+1F)	Unusable		

Table 3.1 List of Input/output Signals

*1 The signal contents will differ when A68ADC Version B and A2CCPU Version B are combined.
For details, refer to Appendix 1. For information on how to read the version, refer to Appendix 2.

REMARK

A/D conversion ready is established when digital output data is stored in the buffer memory after A/D conversion is completed once on all of 8 channels.

IMPORTANT

Devices Y(n+0) to Y(n+3), Y(n+6), Y(n+8) to Y(n+1F) are unusable since they are used in the system.
If any of these devices are used (ON/OFF) in the sequence program, functions of the A68ADC are not guaranteed.

The input and output signals for controlling the A68ADC are in the range of X(Y)n + 0 to X(Y)n + 1F, occupying 4 stations (32 points). Each station number is assigned in units of 8 points, and stations can be set from No. 1 to No. 64.
Table 3.3 shows input/output signal numbers and corresponding station numbers.

Station No.	Input/Output No.	Station No.	Input/Output No.	Station No.	Input/Output No.	Station No.	Input/Output No.
1	X/Y0~7	17	X/Y80~87	33	X/Y100~107	49	X/Y180~187
2	X/Y8~F	18	X/Y88~8F	34	X/Y108~10F	50	X/Y188~18F
3	X/Y10~17	19	X/Y90~97	35	X/Y110~117	51	X/Y190~197
4	X/Y18~1F	20	X/Y98~9F	36	X/Y118~11F	52	X/Y198~19F
5	X/Y20~27	21	X/YA0~A7	37	X/Y120~127	53	X/Y1A0~1A7
6	X/Y28~2F	22	X/YA8~AF	38	X/Y128~12F	54	X/Y1A8~1AF
7	X/Y30~37	23	X/YB0~B7	39	X/Y130~137	55	X/Y1B0~1B7
8	X/Y38~3F	24	X/YB8~BF	40	X/Y138~13F	56	X/Y1B8~1BF
9	X/Y40~47	25	X/YC0~C7	41	X/Y140~147	57	X/Y1C0~1C7
10	X/Y48~4F	26	X/YC8~CF	42	X/Y148~14F	58	X/Y1C8~1CF
11	X/Y50~57	27	X/YD0~D7	43	X/Y150~157	59	X/Y1D0~1D7
12	X/Y58~5F	28	X/YD8~DF	44	X/Y158~15F	60	X/Y1D8~1DF
13	X/Y60~67	29	X/YE0~E7	45	X/Y160~167	61	X/Y1E0~1E7
14	X/Y68~6F	30	X/YE8~EF	46	X/Y168~16F	62	X/Y1E8~1EF
15	X/Y70~77	31	X/YF0~F7	47	X/Y170~177	63	X/Y1F0~1F7
16	X/Y78~7F	32	X/YF8~FF	48	X/Y178~17F	64	X/Y1F8~1FF

Table 3.3 Input/output Signal Numbers and Corresponding Station Numbers

Example) The I/O numbers of controlling I/O signals when the A68ADC is set at station 5.

〈 I/O No. of A68ADC 〉		〈 I/O No. viewed from the PC CPU 〉
X/Y(n + 0)		X/Y20
to	⇨	to
Y/Y(n + 1F)		Y/Y3F

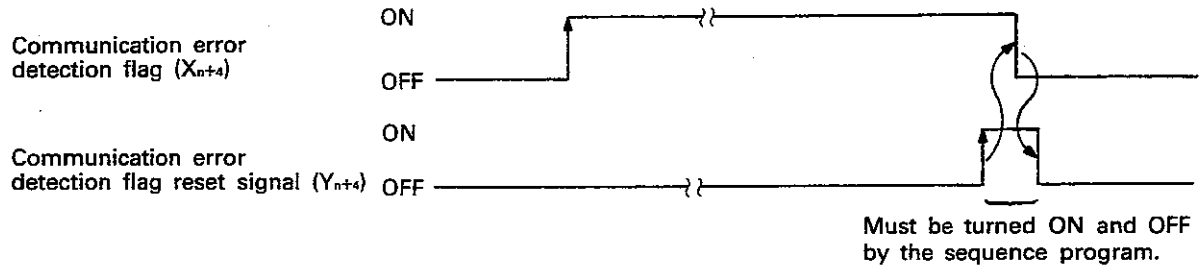
(1) Communication error detection flag (X_{n+4}) and communication error reset signal (Y_{n+4})

Turns ON (latched) when instruction data which cannot be read or written from the A2CCPU to the A68ADC is written. (The RUN LED of the A68ADC flickers.)

When X_{n+4} has turned ON, its error code (see Table 7.1 in Section 7.1) is stored in the error code storage area (special registers D9180 to D9193 of the A2CCPU) of corresponding remote terminal No.

To restart communication, turn ON the communication error reset signal (Y_{n+4}) with the sequence program or, after resetting the A2CCPU, write "0" to address 18 of A68ADC to reset the A68ADC. Then the RUN LED illuminates.

When the communication error reset signal (Y_{n+4}) has turned ON, the error code in the error code storage area (D9180 to D9193) and corresponding FROM/TO instruction information stored in the communication request register area are cleared. (Also see (4) in this section.)



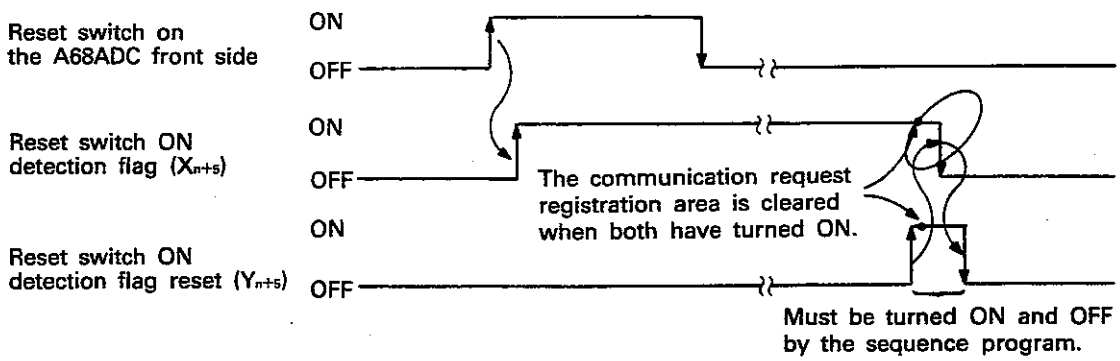
(2) Reset switch ON detection flag (X_{n+5}) and reset switch ON detection flag reset signal (Y_{n+5})

Turns ON (latched) when the reset switch of the A68ADC is moved to reset.

When both the reset switch ON detection flag and the reset switch ON detection flag reset signal have turned ON, the FROM/TO instruction information, stored in the communication request register area, with respect to corresponding remote terminal module is cleared.

However, if the retransmission request signal (Y_{n+7}) is ON, the communication request register area is not cleared.

To restart communication, turn ON the reset switch ON detection flag reset signal (Y_{n+5}) with the sequence program or reset the A2CCPU.

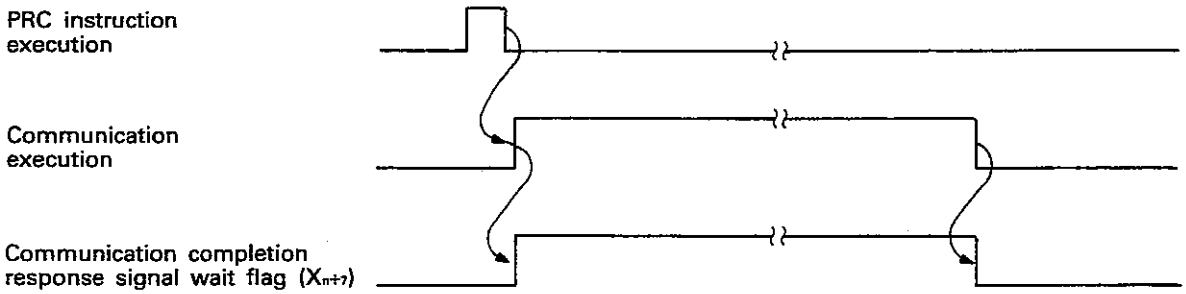


Point

(1) If the A68ADC is reset by moving the reset switch, it returns to the initial state. Start operation with initial setting.

(2) Since (X_{n+5}) turns ON also after the power is turned on, be sure to turn ON (Y_{n+5}) and OFF (X_{n+5}) at the initial stage. And then, execute programs for the A68ADC.

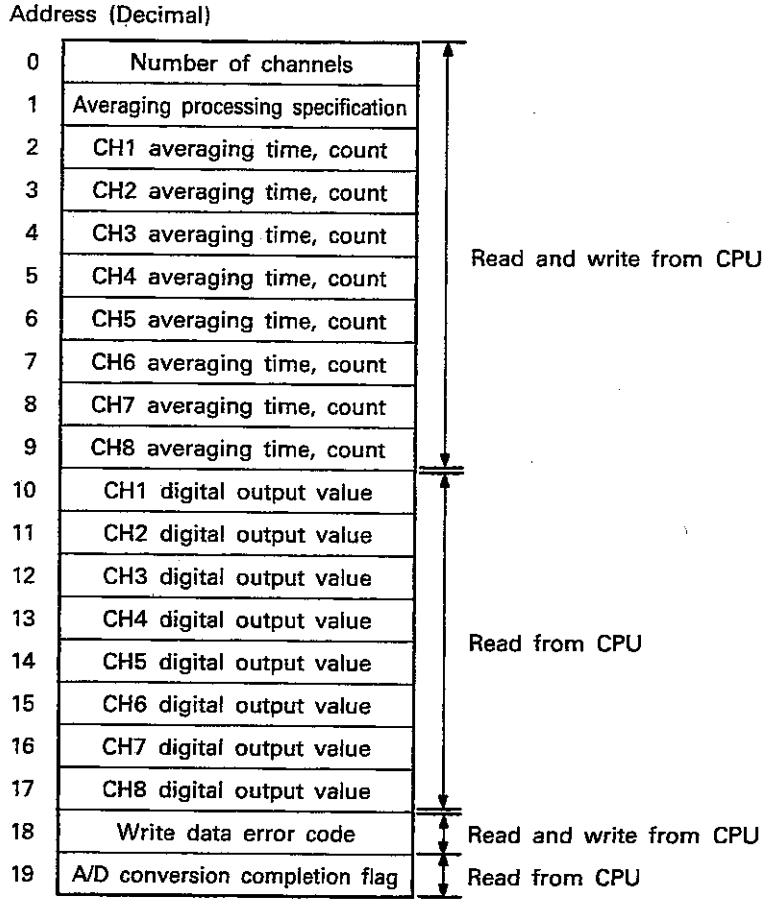
(3) Communication completion response signal wait flag (X_{n+7})
Turns ON when communication with the A68ADC is started by execution of the PRC instruction, and turns OFF when the communication completion response signal from the A68ADC is received.
Turns OFF also when the communication error reset signal (Y_{n+4}) has turned ON.



(4) Communication reset signal (Y_{n+7})
If, for any reason, there is no communication completion response signal for data transmitted by the PRC instruction, A68ADC and A2CCPU are reset to the initial state by setting the communication reset signal (Y_{n+7}) to on.
This only resets the communication state to the initial mode; it does not clear the data that has been set.

3.4 Assignment of Buffer Memory

Assignment of the A68ADC buffer memory (without battery backup) is shown below.



*All 16-bit data.

POINT

Addresses 10 to 17 and 19 of the buffer memory are areas exclusively used for reading from the PLC CPU. Because the A68ADC overwrites digital data in these areas always destroying the buffer memory data. In this case, the A68ADC detects an error, stores the error code in address 18 and flickers the RUN LED.

3.4.1 Contents and data configuration of the buffer memory

(1) Channel designation (Address 0)

(a) At power on, channel designation is set at "00FF$_H$ (255)" for A/D conversion on all channels.

(b) In order to reduce sampling time, channel designation can be changed by the sequence program.

(c) For channel designation change, A/D conversion must be set by each channel.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	–	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Ignored

Channel designation
1: A/D conversion enable
0: A/D conversion disable
Default is "1" for all channels.

(Example) To designate channels 1, 2 and 3 for A/D conversion:
By writing 000D$_H$ (13) to designate channels for A/D conversion, sampling time is obtained as 2.5 msec × 3 = 7.5 msec.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
								CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

➡ 000D$_H$(13)

(2) Averaging processing designation (Address 1)

(a) When the power is turned on and the A/D conversion ready signal of A68ADC is on, all channels are set to sampling processing.

(b) For selection of sampling processing or averaging processing use address 1 of the buffer memory.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Specification of channel for which averaging processing will be performed
1: Averaging processing
0: Sampling processing

Specification of time/count
1: Time averaging
0: Count averaging

POINT

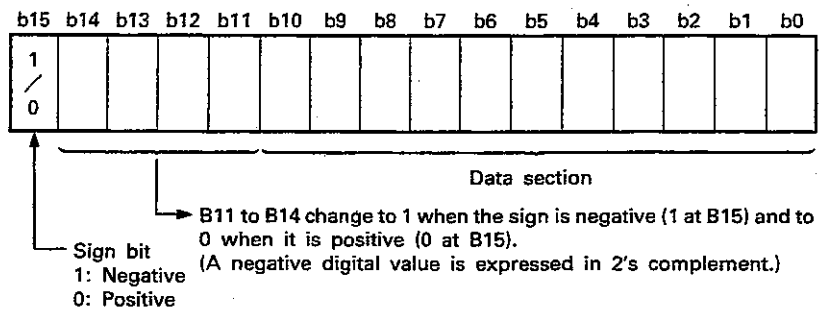
When averaging processing is not specified, sampling processing is set without regard to the specification of time/count.

(3) Averaging time, averaging count (Addresses 2 to 9)
a) At power-on, the averaging time and averaging count are set to 0.
b) The setting ranges are as indicated below:
Averaging processing in terms of count: 1 to 4000 times
Averaging processing in terms of time: 20 to 10000 ms

POINT

If a value outside the above range has been written, setting error occurs and the buffer memory is rewritten. However, the A68ADC performs A/D conversion processing at the averaging time or count previously set.

(4) Digital output value (Addresses 10 to 17)
The digital output value is expressed in 16-bit, signed binary within the range from −2048 to +2047.



(5) Write data error code (Address 18)
a) When data is read from the PLC CPU, the A68ADC makes a data range check for the number of channels, averaging count and averaging time and also performs read/write area access check only once. If any value is outside the range, the A68ADC stores the error code in 16-bit binary. For details of error codes, see Section 7.1.
b) To reset an error code, write 0 from the programmable controller CPU.
c) When several error codes have occurred, the data error code, which has been detected by the A68ADC first, is stored. The other errors are not stored.
d) If an error is reset without remedying the error, the data error code is set to 0 and the RUN LED of A68ADC stops flickering.

(6) A/D conversion completion flag (Address 19)

(a) The A/D conversion completion flag is set to 1 when the A/D conversion ready signal (X1) is turned ON after power on.
When the A/D conversion ready signal has turned ON, A/D conversion on all of 1 to 8 channels is completed, and $00FF_H$ (255) is stored in the buffer memory.

(b) The A/D conversion completion flag processing after power on is performed only once when channel designation for A/D conversion (address 0) is changed.

- Channel designation change from 0 to 1:
  (If averaging processing has been designated, averaging processing of averaging count or time is completed, and then, the A/D conversion digital values are stored in the buffer memory. And, the flag is set to 1.)
- Channel designation change from 1 to 0:
  The A/D conversion completion flag of corresponding channel is set to 0.

(c) The A/D conversion completion flag is provided to each channel.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Channel designation
1: A/D conversion completed.
0: A/D conversion not completed.

(d) The A/D conversion completion flag can be used for the interlock when reading the digital value of the channel for which averaging processing is executed.

3.5 Programming

This section describes the programming procedures when the A68ADC is used as a remote terminal of the A2CCPU.

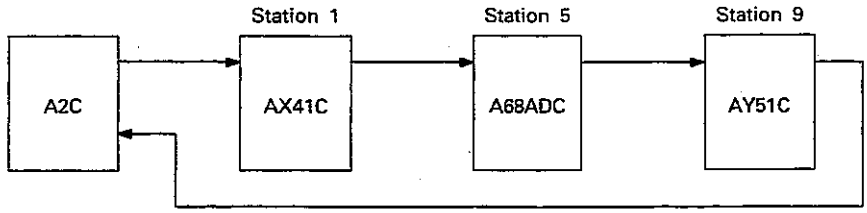
3.5.1 Initial setting of the A2CCPU

The A2CCPU allows connection of up to 14 remote terminals such as A68ADC modules. In order to use those remote terminals, it is necessary to set the remote terminal information in the A2CCPU in the initial setting.
This setting procedure varies with the system disk such as SW4GP-GPPA, SW1S-GPPA and the previous type used for booting. Table 3.2 shows the setting procedures including contents of setting and the differences between types of system disks.

Item	Setting range	Contents	Procedures	
			SW4GP-GPPA SW1S-GPPA	Previous type system FD
Total number of stations	1 to 64	Set the total number of stations including remote I/O modules and remote terminal modules.	Parameter setting	D9036
Head station number	1 to 61	Set the station number (head station number) set with the station number setting switch of each remote terminal module. (Example) A68ADC: Set station number No. 1 AD61C: Set station number No. 5 No. 1 remote terminal module = 1 No. 2 remote terminal module = 5	Parameter setting	D9012: No. 1 remote terminal module D9022: No. 2 remote terminal module D9023: No. 3 remote terminal module D9034: No. 14 remote terminal module
Protocol	0 to 1	Set the protocol used for data communication with remote terminal modules. 0: MINI standard protocol 1: No protocol Must be set at "0".	Parameter setting	D9035
Mode	0 to 2	Set the processings after line error return and at occurrence of line error. 0: Automatic online return enable 1: Automatic online return disable 2: Transmission stop at online error	Parameter setting	D9173

Table 3.2 Initial Setting Contents and Procedures

The following is an example program to write the initial setting data when the system is booted with a previous type system disk.

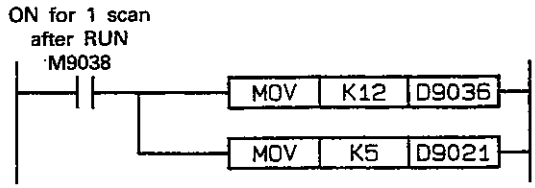


Total number of stations: AX41C: 4 stations
A68ADC: 4 stations
AY41C: 4 stations
4 + 4 + 4 = 12 stations

Head station number: Remote terminal module is A68ADC only.
No. 1 remote terminal: Station 5

Protocol: MINI standard protocol = 0 (default = 0)

Mode: Automatic online return enable = 0 (default = 0)



POINT

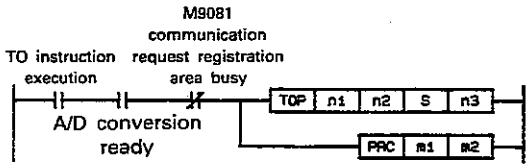
(1) If initial setting data has not been set, an SP. UNIT. ERR. (error No. 46) occurs and the CPU stops operation.

(2) If initial setting is done with both parameters and the sequence program while booting the system with the SW4GP-GPPA or SW1S-GPPA system disk, contents of parameter setting become valid and that set with the sequence program is ignored.

3.5.2 Writing data to the A68ADC

The TO instruction and the PRC instruction are handled as one block of instructions in the sequence program to write data to the buffer memory of designated remote terminal module.
Items to be written and procedures of writing to the A68ADC are described below.

(a) Channel designation
(b) Averaging processing designation
(c) Averaging time and count designation for each channel
(d) Write data error code clear



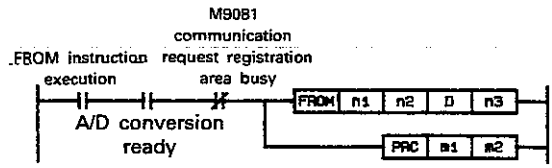
n_1	Head station number of remote terminal module
n_2	Head address of the buffer memory for writing
S	Head number of write data or of device which stores write data.
n_3	Number of write data
m_1	Device number to be turned ON for 1 scan when execution of the TO instruction is completed.
m_2	Dummy device number

For details of instructions, see the ACPU Programming Manual (Common Instructions).

3.5.3 Reading data from the A68ADC

The FROM instruction and the PRC instruction are handled as one block of instructions in the sequence program to read data from the buffer memory of designated remote terminal module.
Items to be read and procedures of reading from the A68ADC are described below.

(a) Digital output of each channel
(b) A/D conversion completion flag
(c) Write data error code

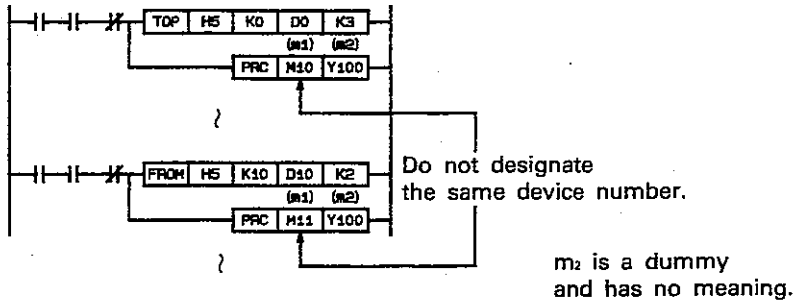


n_1	Head station number of remote terminal module
n_2	Head address of the buffer memory for reading
D	Head number of the device which stores read data.
n_3	Number of read data
m_1	Device number to be turned ON for 1 scan when execution of the FROM instruction is completed.
m_2	Dummy device No.

For details of instructions, see the ACPU Programming Manual (Common Instructions).

3.5.4 Cautions on programming

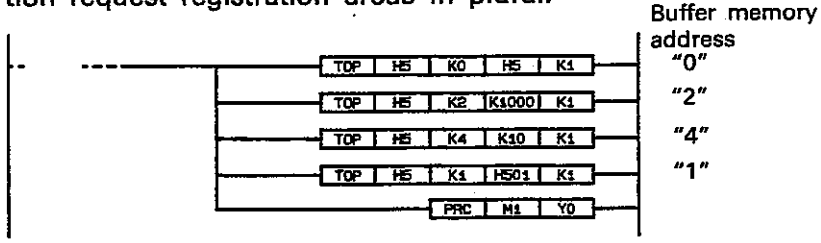
(1) It is necessary to provide the PRC instruction to the step immediately following the FROM/TO instruction. Use care not to designate same devices for "m_1" of the PRC instruction and for "m_1" of the PRC instruction provided to other step.



(2) The communication request registration areas can store up to 32 FROM/TO instructions. If the 33rd FROM/TO instruction is given, it is ignored without processing.
Provide an interlock with M9081 and D9081 so that the FROM/TO instruction may not be executed when the communication request registration areas are full.
M9081 and D9081 are described below.

No.	Contents	Details
M9081	OFF: Communication request registration area has a vacancy. ON: Communication request registration areas are full.	There are 32 communication request registration areas for remote terminals. Turns ON when all areas become full.
D9081	The number of vacant areas of the communication request registration area for remote terminals.	The number of vacant areas of the communication request registration area is stored.

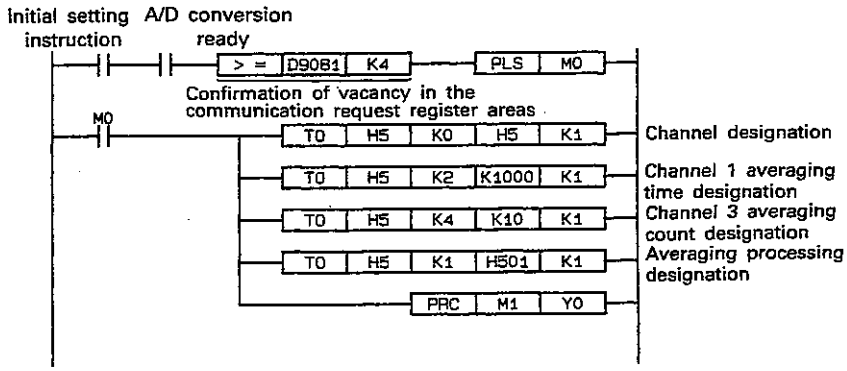
When data is written to two or more addresses in the buffer memory of the A68ADC, one FROM/TO instruction can execute data write if the addresses are continuous. If the addresses are not continuous, it is necessary to execute the FROM/TO instruction at two or more points (see below). In this case, the FROM/TO instruction information is stored in the communication request registration areas in plural.



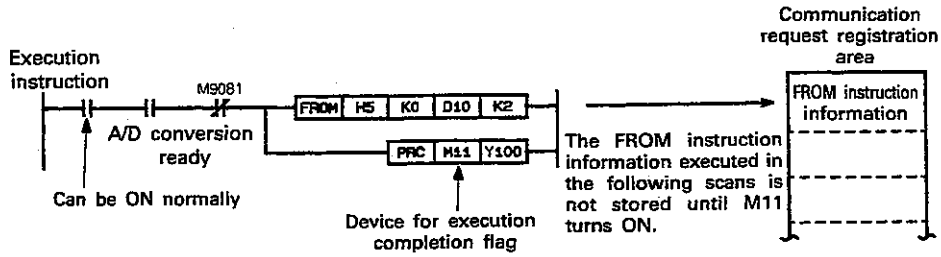
If an attempt is made to store the FROM/TO instruction information which is larger than the number of vacant areas of communication request registration areas, such attempt is ignored. To prevent this, it is necessary to provide a condition to allow confirmation that the vacancy in the communication request registration areas is larger than the number of FROM/TO instruction information. The programming example shown below describes the case when the FROM/TO instruction is executed after confirming the vacancy in the communication request register areas.

Example) Initial setting program for the A68ADC

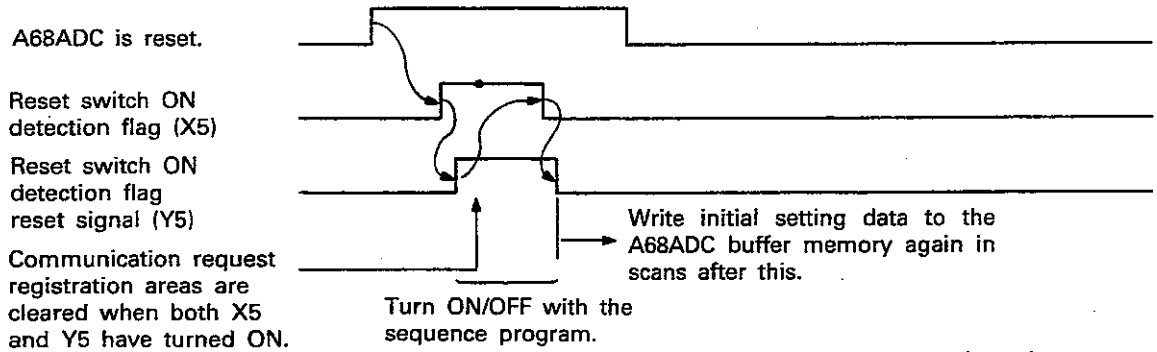
(Channel designation
(buffer memory address 0) Channels 1 and 3
Averaging processing designation
(buffer memory address 1)
Channel 1 averaging processing time
(buffer memory address 2) 1000 msec
Channel 3 averaging processing count
(buffer memory address 4) 10 days)



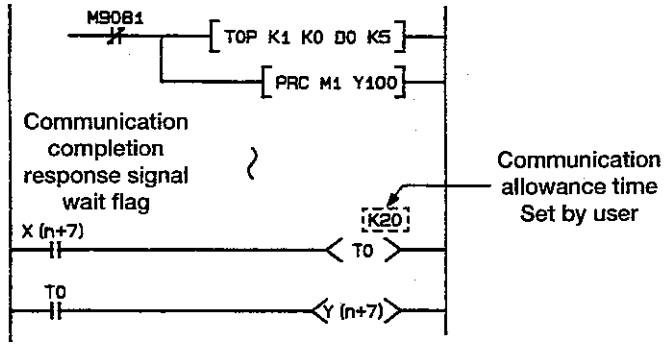
(3) If the execution instruction of the FROM instruction is set to normally ON, the next FROM instruction information is not stored in the communication request registration areas until the processing of the FROM instruction being executed is completed and the execution completion flag designated by the PRC instruction turns ON.
It is not necessary to provide an interlock to allow execution of the FROM instruction after the execution completion flag has turned ON.



(4) When the reset switch on the front of the A68ADC is moved to reset, the A68ADC returns to initial state and performs A/D conversion with defaults.
Monitor the reset switch ON detection flag (X5) with a sequence program and, when the flag has turned ON, write initial setting data again to the A68ADC. (when A/D conversion is executed with other than defaults.)



(5) If a communication completion response signal to the transmission executed to the A68ADC is not sent back, the CPU module is set in the state waiting for the communication completion signal infinitely unless the CPU module is reset. To prevent such a problem, provide a monitoring timer to allow retransmission of the same data at preset time intervals.



Provide the above circuit one block for each remote terminal module.

X (n+7), Y (n+7) are control I/O signals for A68ADC.
For details, refer to Section 3.3

(6) When averaging processing is to be designated for the A68ADC, the data of the number of channels, averaging processing designation, averaging time and averaging count can be written to the buffer memory without restriction when they are written with one TO instruction. If they are written with several TO instructions, follow the order as shown below.

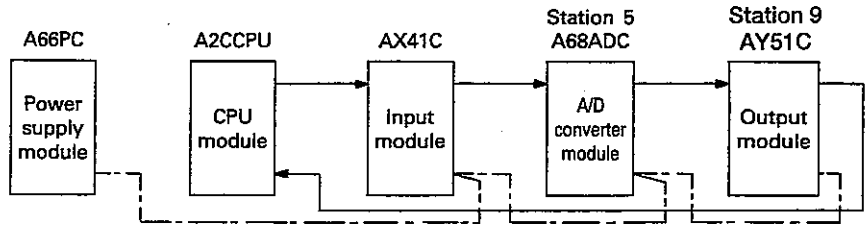
Number of channels → Averaging time or count
→ Averaging processing designation

↑

Must be written last.

3.5.5 Program example

The following is a programming example when the digital output values of channels 1, 2 and 3 of the A68ADC are always read in the system whose configuration is shown below.
Channel 1 is set for averaging by time (500 ms) and channel 2 is set for averaging by count (100 times). Channels 3 to 8 are not set for A/D conversion.



1) I/O numbers (See Section 3.3.)

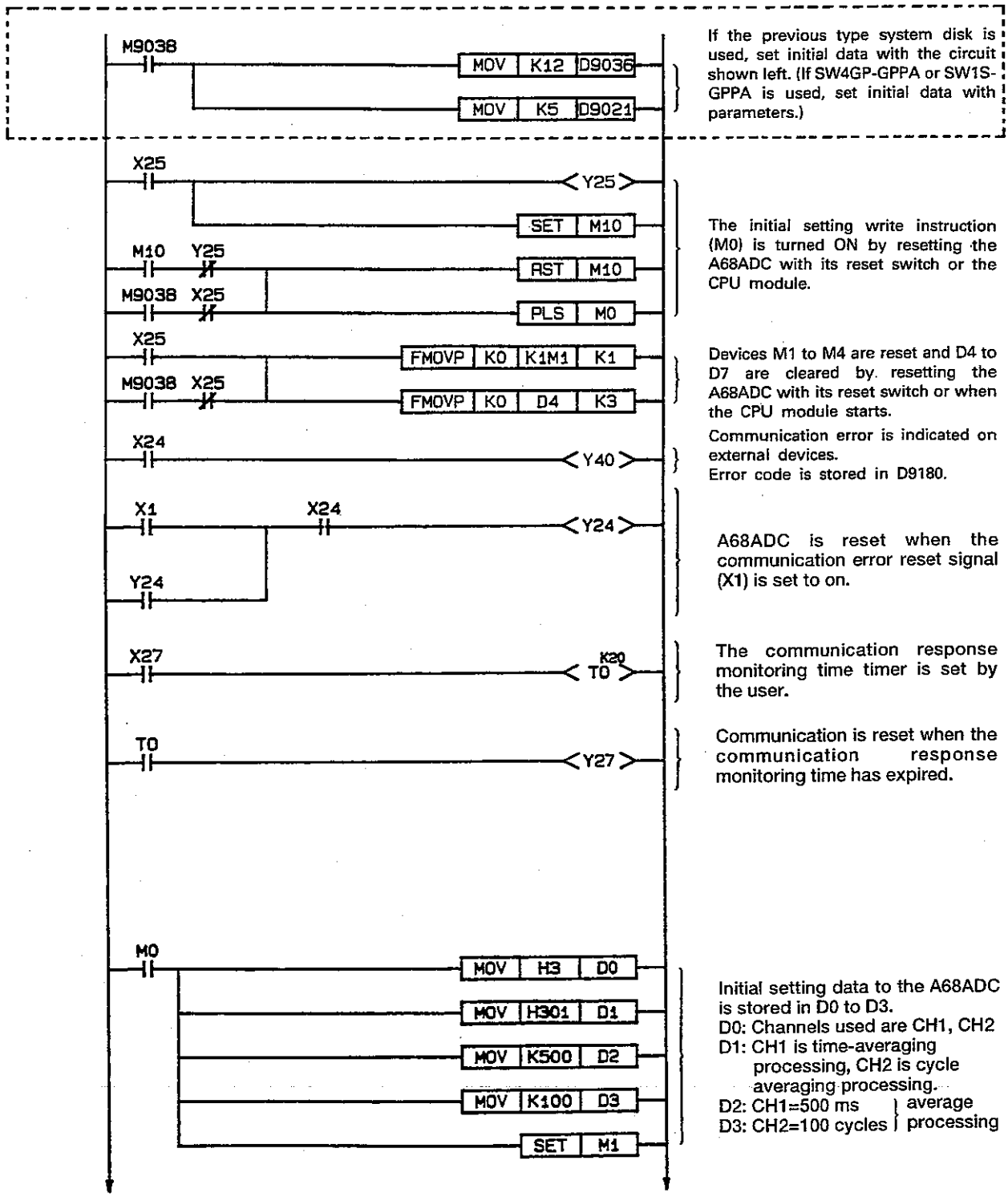
〈 A68ADC I/O numbers 〉		〈 I/O number on CPU side 〉
X/Y(n+0)		X/Y20
to	⇨	to
X/Y(n+1F)		X/Y3F

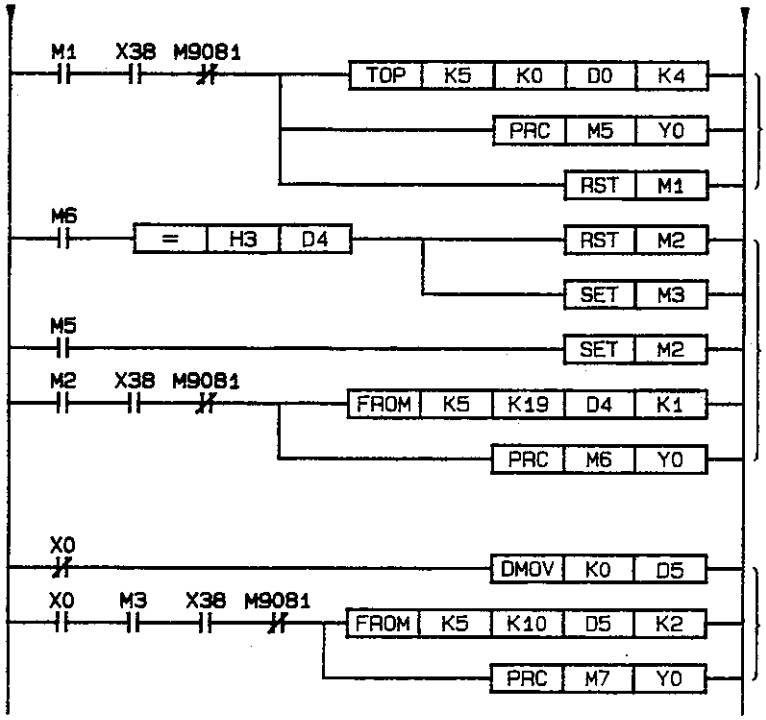
2) A2CCPU remote terminal setting (parameters)
(See Section 3.5.1.)
Total number of stations : 12 stations
Head station number : No. 1 remote terminal module = Station 5
Protocol : MINI standard protocol
Mode : Automatic online return enable

3) Programming
- A/D conversion starts as the CPU module starts. When X0 (read start instruction) of the input module is turned ON, digital outputs are stored in D5 and D6.
- If a communication error between a remote terminal module is detected, Y0 (Y40) of the output module is turned ON to stop all processings.
  When X1 (communication error detection flag reset) is turned ON, the error code storage areas and flags are all cleared.
- When the A68ADC is reset with the reset switch, all processings are stopped. When X2 (reset switch ON detection flag reset) is turned ON, all flags are cleared.

REMARK

Refer to the program example in Appendix 2 for combining the operating times of A68ADC Version B and A2CCPU Version B
The conditions are the same as shown above.


M9038
MOV K12 D9036
MOV K5 D9021
If the previous type system disk is used, set initial data with the circuit shown left. (If SW4GP-GPPA or SW1S-GPPA is used, set initial data with parameters.)
X25
Y25
SET M10
M10 Y25
RST M10
M9038 X25
PLS M0
The initial setting write instruction (M0) is turned ON by resetting the A68ADC with its reset switch or the CPU module.
X25
FMOVP K0 K1M1 K1
M9038 X25
FMOVP K0 D4 K3
Devices M1 to M4 are reset and D4 to D7 are cleared by resetting the A68ADC with its reset switch or when the CPU module starts.
X24
Y40
Communication error is indicated on external devices.
Error code is stored in D9180.
X1
X24
Y24
Y24
A68ADC is reset when the communication error reset signal (X1) is set to on.
X27
K20
T0
The communication response monitoring time timer is set by the user.
T0
Y27
Communication is reset when the communication response monitoring time has expired.
M0
MOV H3 D0
MOV H301 D1
MOV K500 D2
MOV K100 D3
SET M1
Initial setting data to the A68ADC is stored in D0 to D3.
D0: Channels used are CH1, CH2
D1: CH1 is time-averaging processing, CH2 is cycle averaging processing.
D2: CH1=500 ms } average
D3: CH2=100 cycles } processing



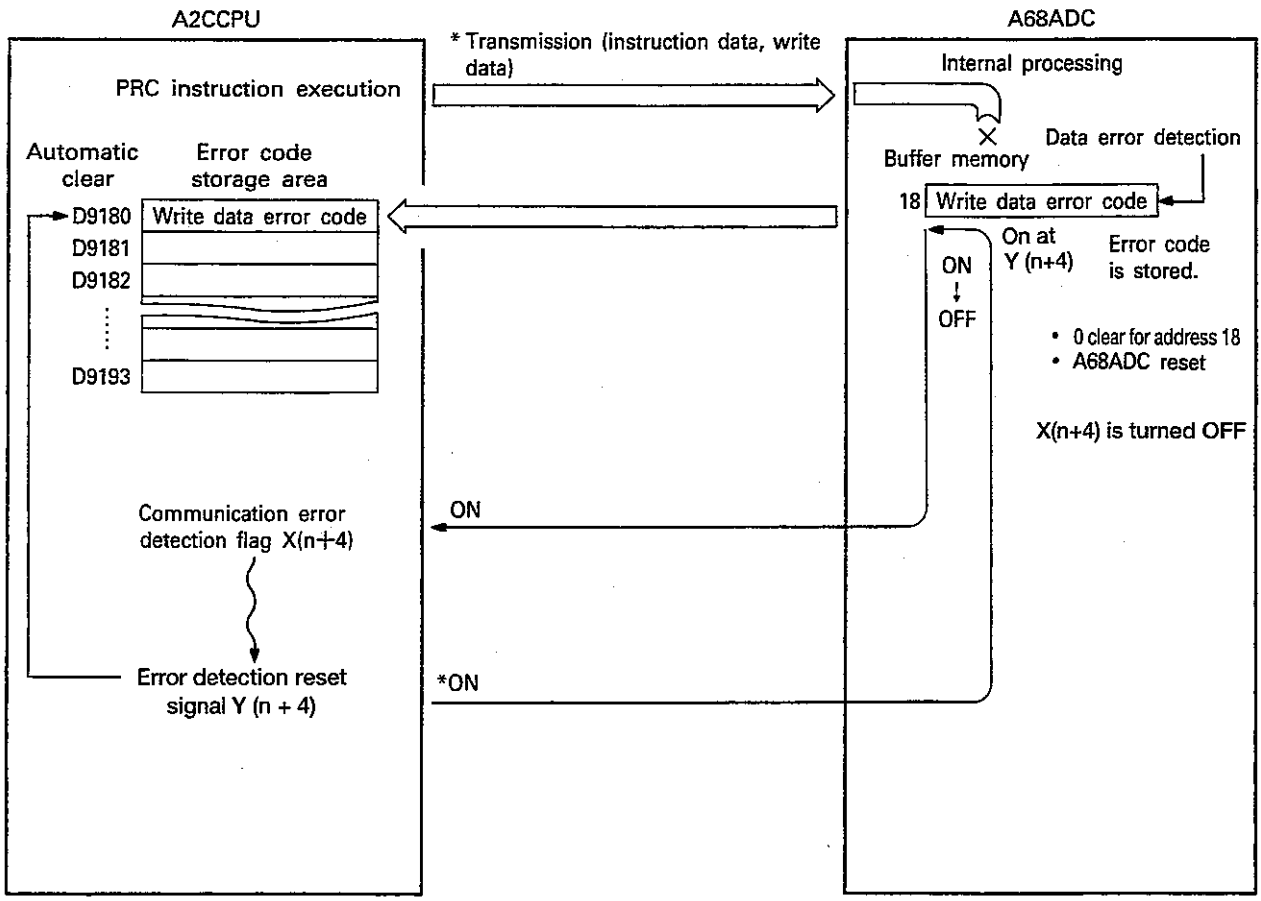
Initial setting data stored in D0 to D3 are written to addresses 0 to 3 of the A68ADC buffer memory.

After writing initial setting data to the A68ADC, the A/D conversion completion flag is read from address 19 of the buffer memory.
When A/D conversion is completed (3H) on both CH1 and CH2, reading of A/D conversion completion flag is stopped and digital output read permission (M3) is turned ON.

When the digital output read instruction (X0) has turned ON, digital output values of CH1 and CH2 are read to D5 and D6.

3.6 Error Detection

The figure below shows how an error is detected when the A2CCPU and the A68ADC are used together.



*Processings marked by an asterisk are executed by the sequence program.

4. LINKING TO THE AnACPU AND THE AJ71PT32-S3

This section gives the linking procedures when dedicated instructions to the MELSECNET/MINI-S3 (master station is AJ71PT32-S3) of the AnACPU are used and the communication of control I/O signals with the A68ADC is set for automatic refresh.
Use the SW4GP-GPPA or SW1S-GPPA system disk for booting.

IMPORTANT

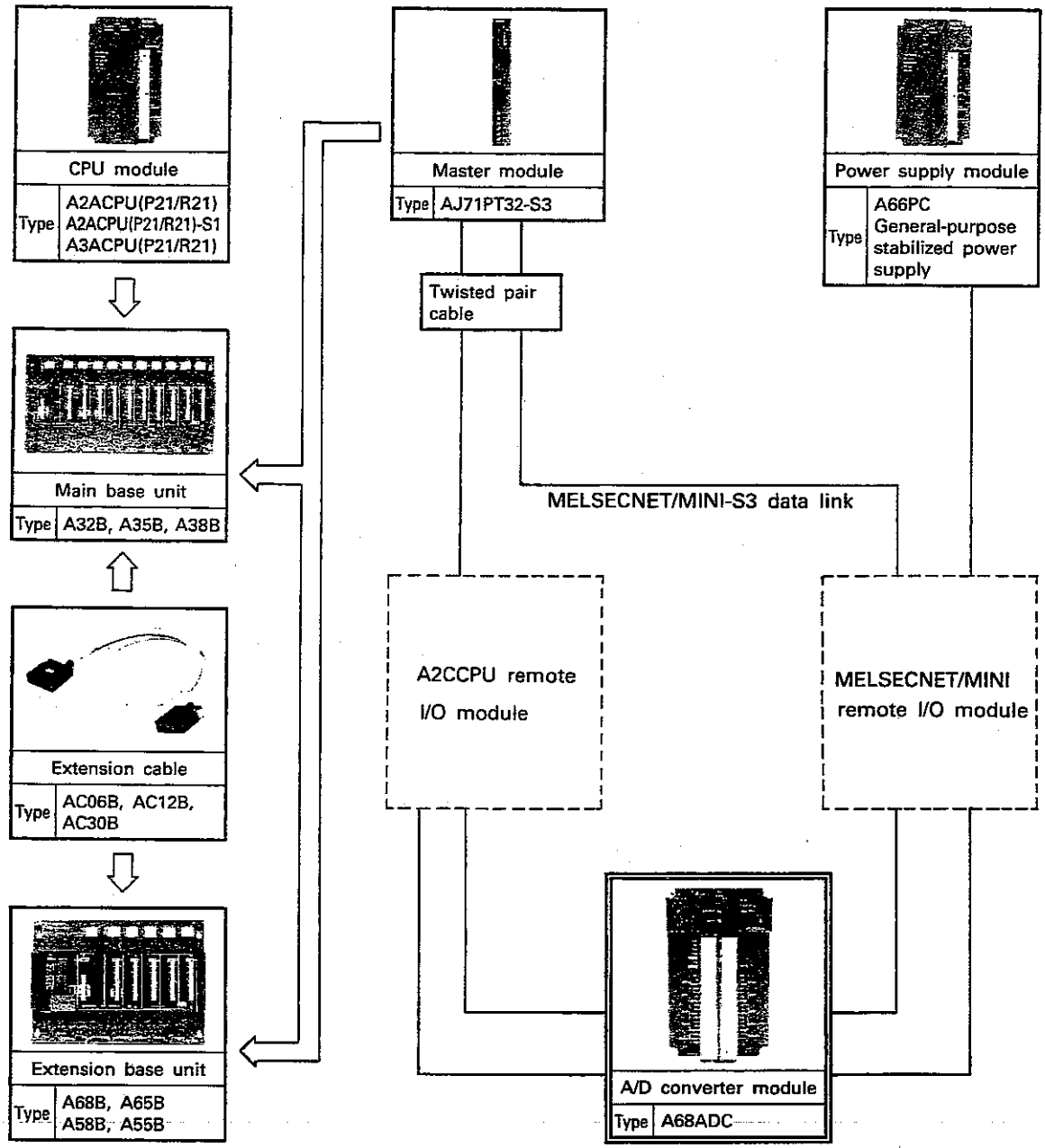
If dedicated instructions are used, the communication of control I/O signals with the A68ADC must be set for automatic refresh.

The linking procedures when dedicated instructions are not used are the same as those when a CPU other than the AnACPU is used. See Section 5 for details.

4.1 System Configuration

The following diagram shows when the A68ADC is used as a remote terminal module of the MELSECNET/MINI-S3 with the AJ71PT32-S3 master module linked to the A2ACPU, A2ACPU-S1 or A3ACPU.

4.1.1 Overall configuration



4.1.2 Applicable system modules

The A68ADC can be used as a remote terminal module of the MELSECNET/MINI-S3 link with the AJ71PT32-S3 as its master module.

(1) A maximum of 14 remote terminal modules such as the A68ADC can be connected to an AJ71PT32-S3 module. The following types of modules are used as remote terminal modules.
- A68ADC (analog/digital converter module)
- AD61C (high speed counter module)
- A64DAVC (digital/analog voltage converter module)
- A64DAIC (digital/analog current converter module)
- AJ35PTF-R2 (RS232C interface module)
- AJ35PT-OPB-MI (mounting type operation box)
- AJ35T-OPB-PI (portable type operation box)

(2) Remote modules connected to the AJ71PT32-S3 can occupy up to 64 stations.

(3) The AJ71PT32-S3 can be connected to an independent CPU system or to the master station or a local station of the MELSECNET data link system. It cannot be connected to a remote I/O station.
The number of modules connected to one CPU module is not limited.

REMARK

For details of the MELSECNET/MINI-S3 link system, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

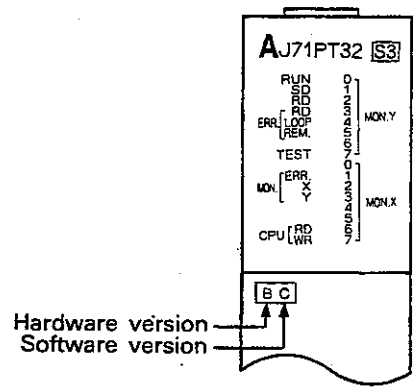
4.1.3 Cautions on constructing the system

(1) Twisted pair cables are used for connection between the AJ71PT32-S3 (master module) and the A68ADC.
The maximum connecting distance between stations varies with cable size when twisted pair cables are used.

0.2 mm² to smaller than 0.5 mm² ····· 50 m
0.5 mm² and larger ····· 100 m

(2) The A68ADC requires external supply of 24 VDC power for internal power supply. Use the A66PC power supply module or a general-purpose stabilized power supply (24 VDC). If one power supply is connected to two or more A68ADC or remote I/O modules, select proper cables and wiring route considering voltage drop due to cables.
Refer to Section 3.1.2 (3) for calculation of voltage drop.

(3) The AJ71PT32-S3 (master module) that can use A68ADC is one that has software version "C" or later shown on the front of the module.
Note that software versions "A", "B" are shown on the front of the master module, or when no version is shown, the AJ71PT32-S3 cannot be used.



IMPORTANT

Use the AJ71PT32-S3 (master module) in the extension mode (48 occupied points). Be sure to mount the initial data ROM storing the total number of remote stations and remote terminal data (set station numbers of remote terminal modules and corresponding remote terminal numbers) to the master module.

4.2 Data Communication Processings

4.2.1 Communication processes

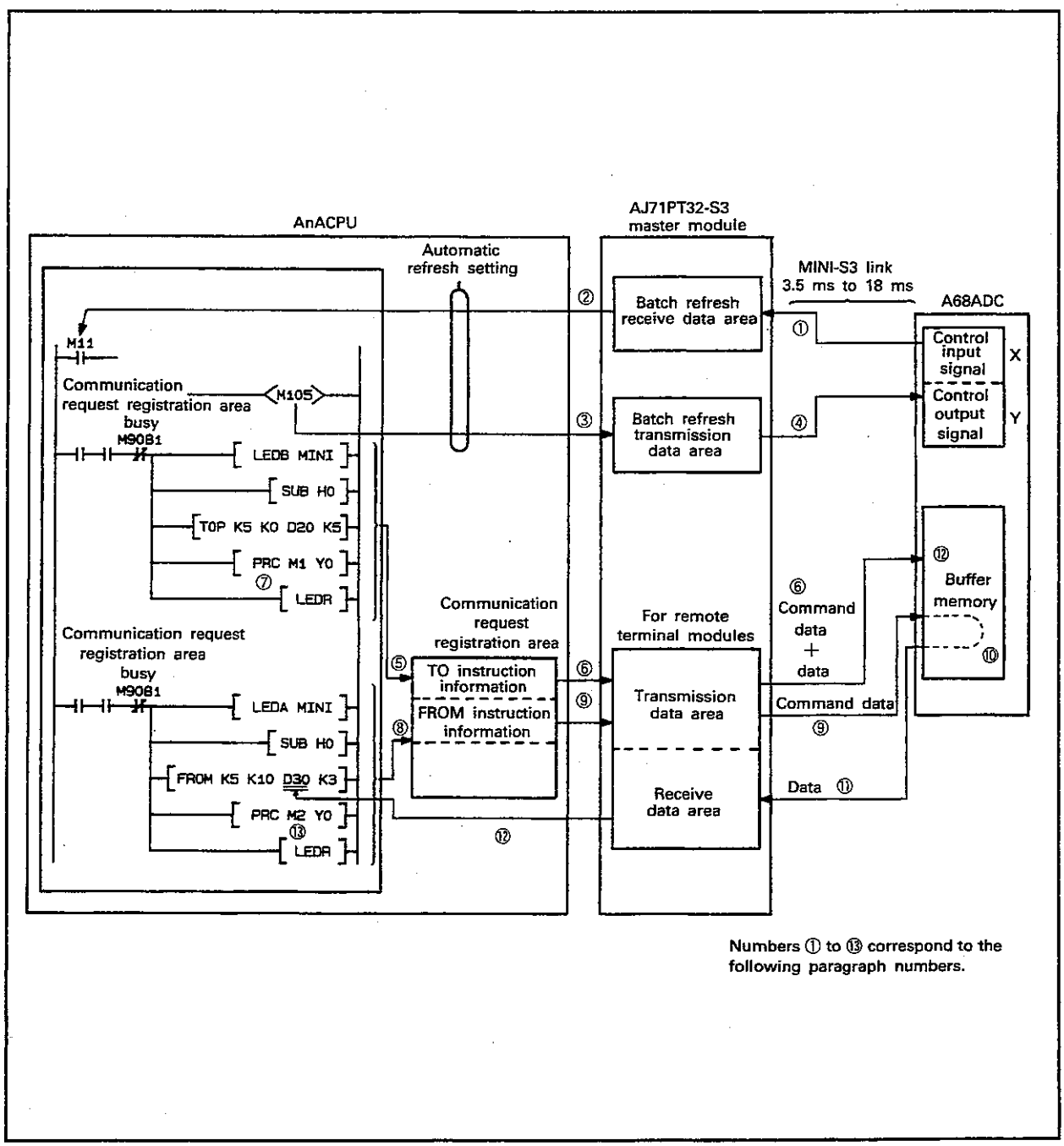


Fig. 4.1 Communication Procedures

(1) Communication processes of control input/output signals used for interlocking of the A68ADC and the AnACPU

① Control input signals from the A68ADC are stored automatically in the batch refresh receive data area in the master module at 3.5 to 18 msec intervals.

② Control input signals stored in the batch refresh receive data area are refreshed to the receive data storage devices as set with parameters.

③ The transmit data storage device ON/OFF information set by automatic refresh setting of parameters is automatically refreshed to the batch refresh transmission data area.

④ Control output signals stored in the batch refresh transmission data area are transmitted to the A68ADC at 3.5 to 18 msec intervals.

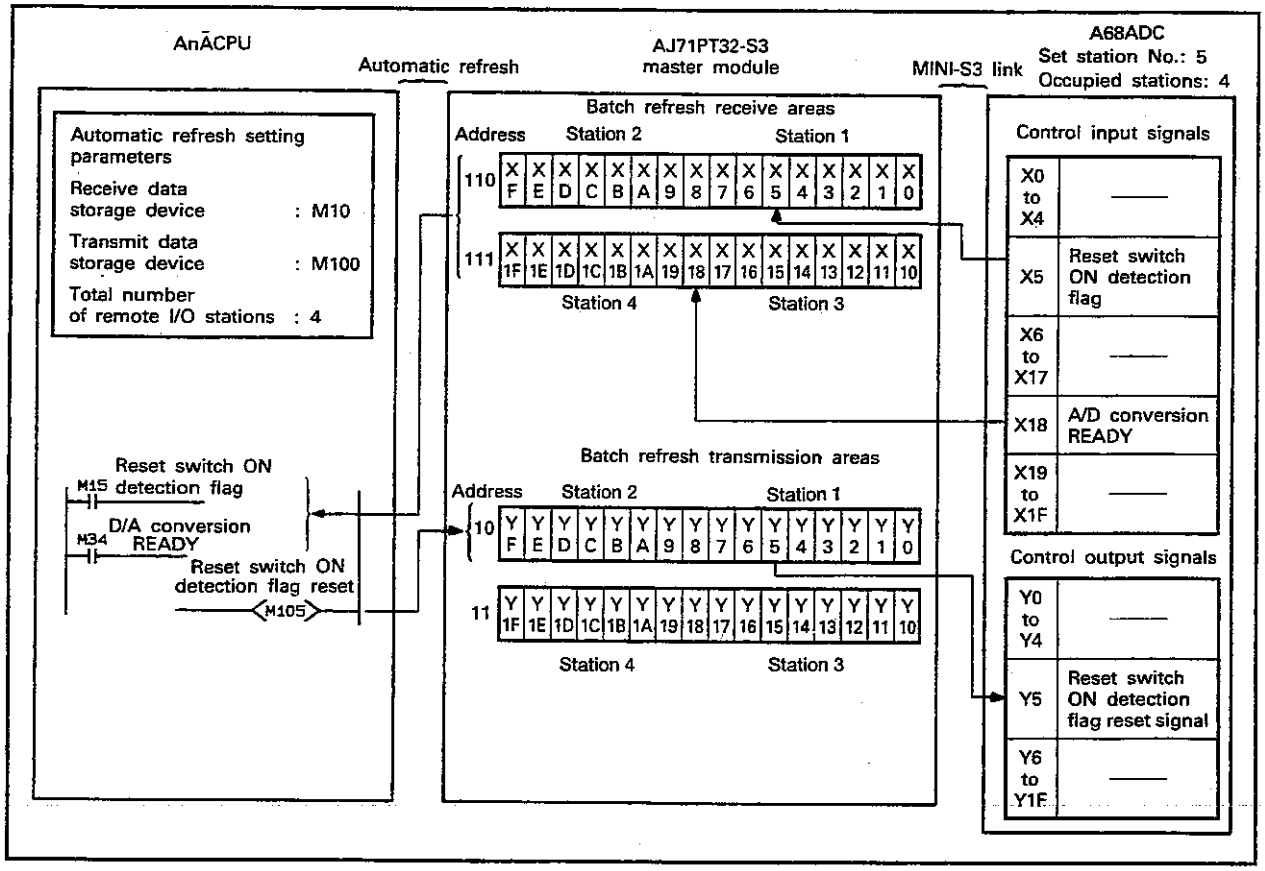


Fig. 4.2 Communication of Control I/O Signals

If automatic refresh is set, it is not necessary to use the FROM/TO instructions for data communication between the PLC CPU and the batch refresh transmission/receive areas of the master modules.

POINT

For details of automatic refresh of the MINI-S3 link, read Section 3.6 "MELSECNET/MINI-S3 Automatic Refresh" of A2A(S1)/A3ACPU User's Manual (Control Functions).

(2) Writing data to the A68ADC buffer memory

⑤ By execution of the "LEDB MINI - TO" instruction (MINI-S3 dedicated instructions) of the sequence program, information such as master module I/O addresses, A68ADC station setting, buffer memory addresses and write instruction commands is stored in the communication request registration areas.

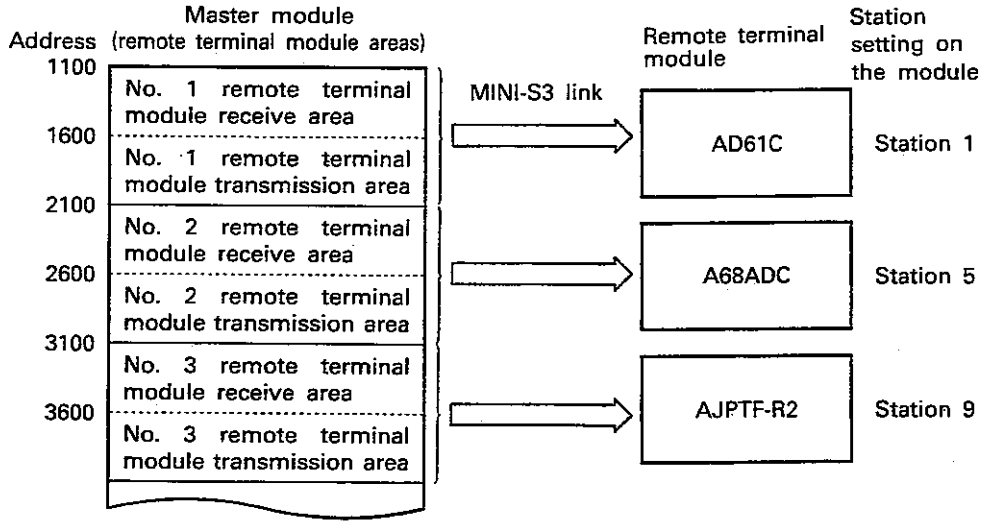
⑥ By execution of the PRC instruction, transmission data is written to the remote terminal module transmission data areas in the master module according to the TO instruction information stored in the communication request registration area. When the data write is completed, the data is transmitted to the A68ADC through the MINI-S3 link. This transmission is performed several times. (one word data per one time)

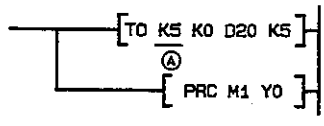
The remote terminal module areas correspond to the remote terminal modules connected to the MINI-S3 link as shown below.

When the initial data stored in the initial data ROM mounted to the master module is as shown right:

No. 1 remote terminal = Station 1
No. 2 remote terminal = Station 5
No. 3 remote terminal = Station 9

See Section 4.5.1 for details of the initial data.





By execution of the program shown left, data for 5 words in D20 is written to the No. 2 remote terminal module transmission area which corresponds to station No. 5 specified by Ⓐ.

⑦ When the transmission completion response of the A68ADC is received by the AnACPU via the receive data areas in the master module, the communication completion flag (device M1 in Fig. 4.1) designated by the PRC instruction turns ON for 1 scan. When communication is completed, the TO instruction information stored in the communication request registration area is cleared.

(3) Reading data from the A68ADC buffer memory

⑧ By execution of the "LEDA MINI to FROM" instruction (MINI-S3 dedicated instructions) of the sequence program, information such as master module I/O addresses, A68ADC station setting, buffer memory addresses and read instruction commands is stored in the communication request registration areas.

⑨ By execution of the PRC instruction, the FROM instruction information stored in the communication request registration area is written to the remote terminal module transmit data areas in the master module. When the information write is completed, the data is transmitted to the A68ADC through the MINI-S3 link. This transmission is performed several times. (one word data per one time)

⑩ When the A68ADC has received the FROM instruction information, it sends data stored in the buffer memory back to the master module according to the address data of the information. (One word data per one time.)

⑪ Data received from the A68ADC is stored in the receive areas of remote terminal numbers corresponding to station setting of the A68ADC.

⑫ Data stored in the remote terminal module receive data areas is stored in the word devices designated by the FROM instruction.

⑬ After storing the data received from the A68ADC buffer memory in the designated devices, the AnACPU turns ON the communication completion flag (device M2 in Fig. 4.1) designated by the PRC instruction for 1 scan. When communication is completed, the FROM instruction information stored in the communication request registration area is cleared.

4.2.2 Processing time

This section introduces the processing time up to the writing of the A68ADC buffer memory data and processing time up to the reading of the data from the buffer memory.

(1) Processing time when writing data.

Maximum processing time
= 3 scan time *1 + tms × (number of write data words + 8)
+40ms *2

(2) Processing time when reading data

Maximum processing time
= 3 scan time *1 + tms × (number of read data words +9)
+40ms *2

*1: The usage time for dedicated commands or partial refresh is 3 --> 1.
*2: A68ADC internal processing time.

"t" is the I/O refresh time and varies with the number and type of connected remote module stations.
The I/O refresh time is calculated as follows.

Mode	Mode Setting	I/O Refresh Time (msec)
Extension mode (48 points)	Automatic return enable (0)	t = 0.66 + (0.044 × R) + (0.25 × B) + (0.95 × T)
	Automatic return disable (1)	t = 0.54 + (0.058 × R) + (0.25 × B) + (0.95 × T)
	Communication stop at error detection (2)	t = 0.54 + (0.051 × R) + (0.25 × B) + (0.95 × T)

R : Total number of remote stations
B : Number of AJ35PTF-128DT modules
T : Number of remote terminal modules

4.3 Input/output Signals Handled With the PC CPU

4.3.1 I/O signals of the A68ADC

Functions of the control input and output signals handled between the A68ADC and AnACPU are described in this section. Devices X refer to the input signals from the A68ADC to the AnACPU. Devices Y refer to the output signals from the AnACPU to the A68ADC.

Signal Direction: A68ADC → AnACPU		Signal Direction: AnACPU → A68ADC	
Device No.	Description	Device No.	Description
X0 to X4	Unusable	Y0 to Y4	Unusable
X5	Reset switch ON detection flag of the A68ADC module		
X6 to X17	Unusable		
X18	A/D conversion ready (1) Turns ON when A/D conversion is ready in the normal mode (other than the test mode) after the power was turned on or the PLC CPU was reset. Turns OFF when mode is switched from normal to test. (2) Used for the interlock for reading and writing from the PLC CPU to the A68ADC.		
		Y5	Reset switch ON detection flag reset signal
X19 to X1F	Unusable	Y6 to Y1F	Unusable

Table 4.1 List of Input/output Signals

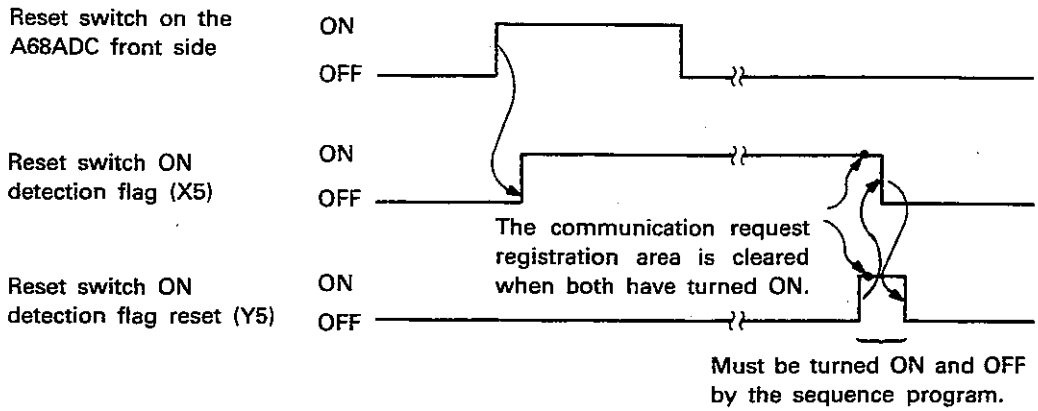
REMARK

A/D conversion ready is established when digital output data is stored in the buffer memory after one time of completion of A/D conversion on all of 8 channels.

IMPORTANT

Devices Y0 to Y4, and Y6 to Y1F are unusable since they are used in the system.
If any of these devices are used (ON/OFF) in the sequence program, functions of the A68ADC are not guaranteed.

(1) Reset switch ON detection flag (X5) and reset switch ON detection flag reset signal (Y5)
Turns ON (latched) when the reset switch of the A68ADC is moved to reset.
When both the reset switch ON detection flag and the reset switch ON detection flag reset signal have turned ON, the FROM/TO instruction information, stored in the communication request registration area, of the corresponding remote terminal module is cleared.
To restart communication, turn ON the reset switch ON detection flag reset signal (Y5) with the sequence program or reset the AnACPU.



POINT

(1) If the A68ADC is reset by moving the reset switch, it returns to the initial state. Start operation from the initial setting.
(2) Since X5 turns ON also after the power is turned on, be sure to turn ON Y5 and OFF X5 at the initial stage. And then, execute program for the A68ADC.

4.3.2 I/O signals of the AJ71PT32-S3

Device No.	Signal Name		Device No.	Signal Name	
X (n+0)	Transmission completion signal	For remote terminal module No. 1	Y (n+0)	Transmission request signal	For remote terminal module No. 1
X (n+1)	Read request signal		Y (n+1)	Read completion signal	
X (n+2)	Transmission completion signal	For remote terminal module No. 2	Y (n+2)	Transmission request signal	For remote terminal module No. 2
X (n+3)	Read request signal		Y (n+3)	Read completion signal	
X (n+4)	Transmission completion signal	For remote terminal module No. 3	Y (n+4)	Transmission request signal	For remote terminal module No. 3
X (n+5)	Read request signal		Y (n+5)	Read completion signal	
X (n+6)	Transmission completion signal	For remote terminal module No. 4	Y (n+6)	Transmission request signal	For remote terminal module No. 4
X (n+7)	Read request signal		Y (n+7)	Read completion signal	
X (n+8)	Transmission completion signal	For remote terminal module No. 5	Y (n+8)	Transmission request signal	For remote terminal module No. 5
X (n+9)	Read request signal		Y (n+9)	Read completion signal	
X (n+A)	Transmission completion signal	For remote terminal module No. 6	Y (n+A)	Transmission request signal	For remote terminal module No. 6
X (n+B)	Read request signal		Y (n+B)	Read completion signal	
X (n+C)	Transmission completion signal	For remote terminal module No. 7	Y (n+C)	Transmission request signal	For remote terminal module No. 7
X (n+D)	Read request signal		Y (n+D)	Read completion signal	
X (n+E)	Transmission completion signal	For remote terminal module No. 8	Y (n+E)	Transmission request signal	For remote terminal module No. 8
X (n+F)	Read request signal		Y (n+F)	Read completion signal	
X (n+10)	Transmission completion signal	For remote terminal module No. 9	Y (n+10)	Transmission request signal	For remote terminal module No. 9
X (n+11)	Read request signal		Y (n+11)	Read completion signal	
X (n+12)	Transmission completion signal	For remote terminal module No. 10	Y (n+12)	Transmission request signal	For remote terminal module No. 10
X (n+13)	Read request signal		Y (n+13)	Read completion signal	
X (n+14)	Transmission completion signal	For remote terminal module No. 11	Y (n+14)	Transmission request signal	For remote terminal module No. 11
X (n+15)	Read request signal		Y (n+15)	Read completion signal	
X (n+16)	Transmission completion signal	For remote terminal module No. 12	Y (n+16)	Transmission request signal	For remote terminal module No. 12
X (n+17)	Read request signal		Y (n+17)	Read completion signal	
X (n+18)	Transmission completion signal	For remote terminal module No. 13	Y (n+18)	Transmission request signal	For remote terminal module No. 13
X (n+19)	Read request signal		Y (n+19)	Read completion signal	
X (n+1A)	Transmission completion signal	For remote terminal module No. 14	Y (n+1A)	Transmission request signal	For remote terminal module No. 14
X (n+1B)	Read request signal		Y (n+1B)	Read completion signal	
X (n+1C)	Unusable		Y (n+1C)	Unusable	
X (n+1D)			Y (n+1D)		
X (n+1E)			Y (n+1E)		
X (n+1F)			Y (n+1F)		
X (n+20)	Hardware error		Y (n+20)		
X (n+21)	MINI-S3 link communicating		Y (n+21)		
X (n+22)	Unusable		Y (n+22)		
X (n+23)	Receive data clear completion		Y (n+23)	Receive data clear request	
X (n+24)	Remote terminal module error detection		Y (n+24)	Remote terminal module error detection reset	
X (n+25)	Test mode		Y (n+25)	Unusable	
X (n+26)	MINI-S3 link error detection		Y (n+26)		
X (n+27)	MINI-S3 link communication error		Y (n+27)		
X (n+28)	ROM error		Y (n+28)	MINI-S3 link communication start	
X (n+29)	Unusable		Y (n+29)	Unusable	
X (n+2A)			Y (n+2A)	FROM/TO instruction response designation	
X (n+2B)			Y (n+2B)	Faulty station data clear designation	
X (n+2C)			Y (n+2C)	Unusable	
X (n+2D)			Y (n+2D)	Error reset	
X (n+2E)			Y (n+2E)	Unusable	
X (n+2F)			Y (n+2F)		

Table 4.2 List of I/O Signals

"n" specifies value of the head I/O address of the AJ71PT32-S3.
Example) When the I/O address of the AJ71PT32-S3 is between X/Y20 and X/Y4F: X (n + 0) to X (n + 2F) = X20 to X4F
Y (n + 0) to Y (n + 2F) = Y20 to Y4F

REMARK

For details of functions and purposes of control I/O signals, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

4.4 Assignment of Buffer Memory

4.4.1 Contents and configuration of the A68ADC buffer memory

Assignment of the A68ADC buffer memory (without battery backup) is shown below.

Address (Decimal)		
0	Number of channels	Read and write from CPU
1	Averaging processing specification	
2	CH1 averaging time, count	
3	CH2 averaging time, count	
4	CH3 averaging time, count	
5	CH4 averaging time, count	
6	CH5 averaging time, count	
7	CH6 averaging time, count	
8	CH7 averaging time, count	
9	CH8 averaging time, count	
10	CH1 digital output value	Read from CPU
11	CH2 digital output value	
12	CH3 digital output value	
13	CH4 digital output value	
14	CH5 digital output value	
15	CH6 digital output value	
16	CH7 digital output value	
17	CH8 digital output value	
18	Write data error code	Read and write from CPU
19	A/D conversion completion flag	Read from CPU

*All 16-bit data.

POINT

Addresses 10 to 17 and 19 of the buffer memory are areas exclusively used for reading from the PLC CPU. Because the A68ADC overwrites digital data in these areas always destroying the buffer memory data. In this case, the A68ADC detects an error, stores the error code in address 18 and flickers the RUN LED.

(1) Channel designation (Address 0)

(a) At power on, channel designation is set at "00FF$_H$ (255)" for A/D conversion on all channels.

(b) In order to reduce sampling time, channel designation can be changed by the sequence program.

(c) For channel designation change, A/D conversion must be set by each channel.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	–	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Ignored

Channel designation
1: A/D conversion enable
0: A/D conversion disable

Default is "1" for all channels.

(Example) To designate channels 1, 3 and 4 for A/D conversion:
By writing 000D$_H$ (13) to designate channels for A/D conversion, sampling time is obtained as 2.5 ms × 3 = 7.5 ms.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
								CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

→ 000D$_H$ (13)

(2) Averaging processing designation (Address 1)

(a) When the power is turned on and the A/D conversion ready signal of A68ADC is on, all channels are set to sampling processing.

(b) For selection of sampling processing or averaging processing use address 1 of the buffer memory.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Specification of channel for which averaging processing will be performed
1: Averaging processing
0: Sampling processing

Specification of time/count
1: Time averaging
0: Count averaging

POINT

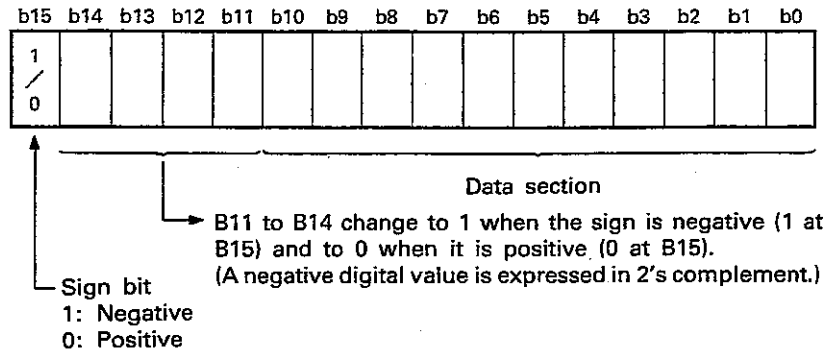
When averaging processing is not specified, sampling processing is set without regard to the specification of time/count.

(3) Averaging time, averaging count (Addresses 2 to 9)
a) At power-on, the averaging time and averaging count are set to 0.
b) The setting ranges are as indicated below:
Averaging processing in terms of count: 1 to 4000 times
Averaging processing in terms of time: 20 to 10000 ms

POINT

If a value outside the above range has been written, setting error occurs and the buffer memory is rewritten. However, the A68ADC performs A/D conversion processing at the averaging time or count previously set.

(4) Digital output value (Addresses 10 to 17)
The digital output value is expressed in 16-bit, signed binary within the range from −2048 to +2047.



(5) Write data error code (Address 18)
a) When data is read from the PLC CPU, the A68ADC makes a data range check for the number of channels, averaging count and averaging time and also performs read/write area access check only once. If any value is outside the range, the A68ADC stores the error code in 16-bit binary. For details of error codes, see Section 7.1.
b) To reset an error code, write 0 from the programmable controller CPU.
c) When several error codes have occurred, the data error code, which has been detected by the A68ADC first, is stored. The other errors are not stored.
d) If an error is reset without remedying the error, the data error code is set to 0 and the RUN LED of A68ADC stops flickering.

(6) A/D conversion completion flag (Address 19)

(a) The A/D conversion completion flag is set to 1 when the A/D conversion ready signal (X1) is turned ON after power on.
When the A/D conversion ready signal has turned ON, A/D conversion on all of 1 to 8 channels is completed, and 00FF$_H$ (255) is stored in the buffer memory.

(b) The A/D conversion completion flag processing after power on is performed only once when channel designation for A/D conversion (address 0) is changed.

- Channel designation change from 0 to 1:
  (If averaging processing has been designated, averaging processing of averaging count or time is completed, and then, the A/D conversion digital values are stored in the buffer memory. And, the flag is set to 1.)

- Channel designation change from 1 to 0:
  The A/D conversion completion flag of corresponding channel is set to 0.

(c) The A/D conversion completion flag is provided to each channel.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Channel designation
1: A/D conversion completed.
0: A/D conversion not completed.

(d) The A/D conversion completion flag can be used for the interlock when reading the digital value of the channel for which averaging processing is executed.

4.4.2 Contents and configuration of the AJ71PT32-S3 buffer memory

The AJ71PT32-S3 is provided with a buffer memory (without battery backup) for data communication with the PLC CPU.
Use the FROM/TO instructions to read and write data from to the buffer memory.

(1) Assignment of the buffer memory

Address (decimal)		Content	Read/write by PLC CPU
0	(Unused)	—	Read/write enable
1	Retry count	Sets the number of retries when communication error has occurred.	
	(Unused)	—	
4	Line error check	Checks location of line error.	
	(Unused)	—	
10 to 41	Batch refresh transmission data	Writes data to be output to the batch refresh type remote I/O module.	
	(Unused)	—	—
70 to 77	Remote module card information	Stores type identification of each remote module being connected.	Read only
	(Unused)	—	—
90 to 93	Accumulated faulty station detection	Stores faulty remote station numbers. (Detected state is retained until reset.)	Read/write enable
	(Unused)	—	—
100 to 103	Faulty station detection	Stores faulty remote station numbers. (Update state is retained.)	Read only
	(Unused)	—	
107	Communication error code	Stores the cause of the MINI-S3 link communication error signal ON.	
108	Error detection code	Stores accumulated count of the MINI-S3 link error detection ON.	
	(Unused)	—	
110 to 141	Batch refresh receive data	Stores the input data from the batch refresh type remote I/O modules.	
	(Unused)	—	
160	Line error retry counter	Stores the number of retries when communication with all remote modules fails due to line error.	
161 to 192	Retry counter	Stores the number of retries executed to faulty stations.	
	(Unused)	—	
195	Remote terminal module faulty station	Stores the station number when a remote terminal module has caused an error.	
196 to 209	Remote terminal module error code	Stores the cause of the remote terminal module error detection signal X(n+24) ON.	
	(Unused)	—	—
250 to 282	Partial refresh station set data	Writes the station number and digit designation (number of time of division) of the partial refresh type remote I/O module.	Read/write enable
	(Unused)	—	
300 to 363	Partial refresh transmission data	Writes data to be output to the partial refresh type remote I/O module.	
	(Unused)	—	
598	Partial refresh accumulated input error detection	Stores the input faulty station number of the partial refresh type remote I/O module input data. (Detected state is retained until reset.)	
599	Partial refresh input error detection	Stores the input faulty station number of the partial refresh type remote I/O module input data. (Update state of communication is stored.)	
600 to 663	Partial refresh receive data	Stores input data of the partial refresh type remote I/O module.	Read only

Address (decimal)		Content	Read/write by PLC CPU
858	Receive data clear designation	Sets the AJ35PTF-R2 station that clears receive data by the receive data clear request signal Y(n+23).	Read/write enable
859	Receive data clear range designation	Designates the receive buffer that clears receive data by the receive data clear request signal Y(n+23).	
860 to 929	No-protocol mode parameter	Sets the parameters when the AJ35PTF-R2 is used in the no-protocol mode.	
930 to 1099	(Unused)	—	—

	(*1) Channel 0	(*1) Channel 1		
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8	Areas to which transmission data to remote terminal modules is written or to store data received from remote terminal modules.	Read/write enable
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9		
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10		
4100 to 5099	Communication area for remote terminal No. 4	Communication area for remote terminal No. 11		
5100 to 6099	Communication area for remote terminal No. 5	Communication area for remote terminal No. 12		
6100 to 7099	Communication area for remote terminal No. 6	Communication area for remote terminal No. 13		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14		

POINT

(1) Channels specified with *1 are used for executing read/write at areas of addresses 1100 to 8099 and are automatically switched according to the remote terminal module station number as designated by the MINI-S3 dedicated instructions.

(2) The buffer memory is all cleard (0 is stored.) at power on or when the PLC CPU is reset. However, retry count (adress 1) and no-protocol mode parameters (addresses 860 to 929) are set at defaults.

(3) Do not write data from the PLC CPU to read only areas.

(4) Unused areas are used by the system of the master module.

(5) Data in the buffer memory can be read continuously including unused areas. For example, data of accumulated faulty stations detection (addresses 90 to 93) and faulty station detection (addresses 100 to 103) can be read by a single FROM instruction.

REMARK

For details of contents at each address and data configuration of the buffer memory, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

(2) Remote terminal communication areas (addresses 1100 to 8099)

(a) Areas for data communication with remote terminal modules.

(b) The communication areas are assigned to two channels. Channel 0 is assigned to remote terminal modules No. 1 to No. 7, and channel 1 is assigned to remote terminal modules No. 8 to No. 14.
Channels are automatically switched according to the remote terminal module station number as designated by the MINI-S3 dedicated instructions.

	Channel 0	Channel 1
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10
4100 to 7099		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14

The remote terminal module number refers to the number assigned to each remote terminal module set in the initial data ROM of the master module.
Data read/write is executed for areas which correspond to the module numbers assigned to each remote terminal module.

(c) Each communication area consists of a transmission area and a receive area. Capacity of each area at power on is 500 words.

Communication area for remote terminal module No. 1

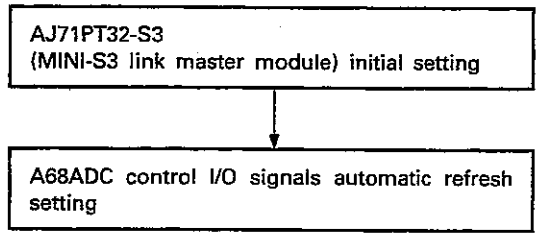
1100 to 1599	Receive area (FROM area)
1600 to 2099	Transmission area (TO area)

The transmission area sets data to be transmitted to remote terminal modules.
The receive area stores data received from remote terminal modules.

(d) Capacity of the transmission and receive areas can be changed by the initial data setting of the master module. (Note that the total capacity of the two areas must not exceed 1000 words.)
Example) Receive area: 200 words, Transmission area: 800 words

4.5 Contents of Initial Setting

The contents of initial setting when the A68ADC is used as a remote terminal module employing the MELSECNET/MINI-S3 dedicated instructions (hereinafter referred to as the MINI-S3 dedicated instructions) for the AnACPU are described.



4.5.1 Initial setting of the AJ71PT32-S3

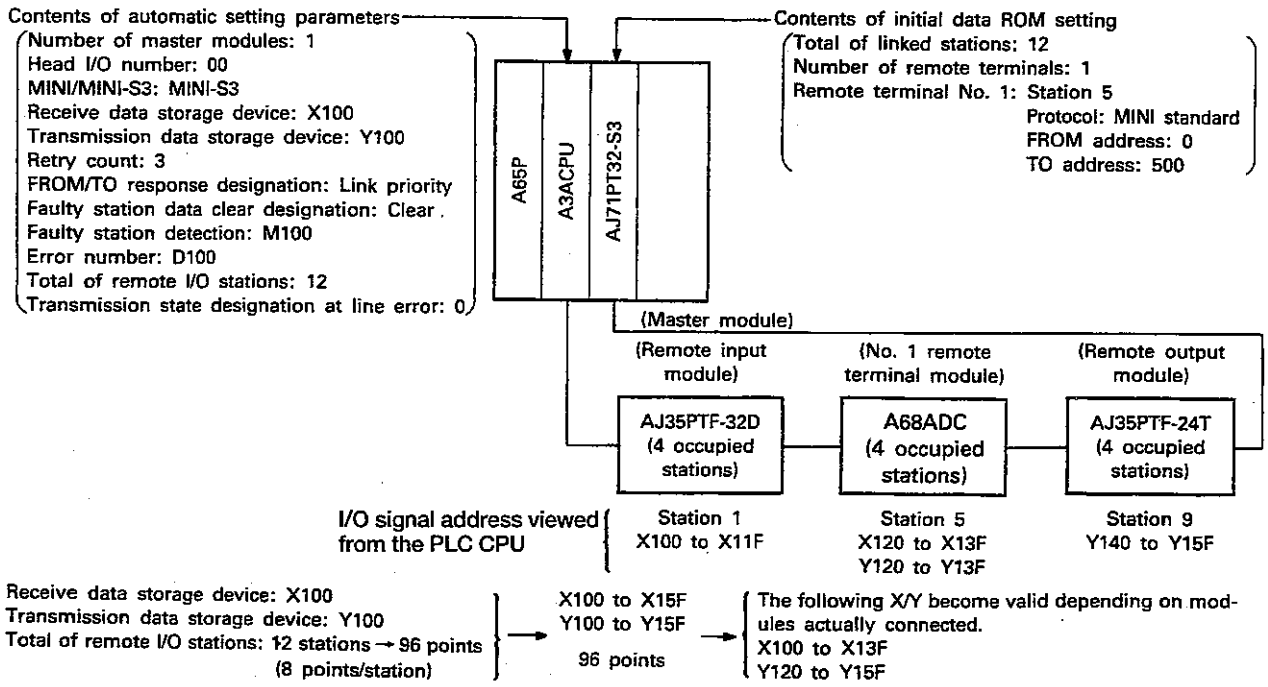
Use the SW□GP-MINIP system disk to set initial data and to store it in the initial data ROM.
The initial data ROM is inserted to the ROM socket of the AJ71PT32-S3.
Contents of initial data setting are mentioned below.

- Total number of remote stations: Set the total number of occupied stations of each module connected to the MINI-S3 link.
  Example) AJ35PTF-32A (remote I/O module) 4 stations
  A68ADC (remote terminal module) 4 stations
  AJ35PTF-24T (remote I/O module) 4 stations
  Total: 12 stations
- Station number of each remote terminal number: Set the station numbers set for modules which correspond to remote terminal modules No. 1 to No. 14.
  Example) AJ35PTF-32A 1 stations
  A68ADC 5 stations ← Remote terminal module
  AJ35PTF-24T 9 stations
  Remote terminal No. 1=5 stations
- Protocol: Set the protocol used for communications with the A68ADC.
  Use the MINI standard protocol.
- Remote terminal FROM/TO area setting: Set the capacity for the FROM area and the TO area as explained in Section 4.4.2 (2).
  Default is 500 words for each of the FROM area and the TO area.

For details of setting procedures, refer to SW□GP-MINIP Operating Manual.

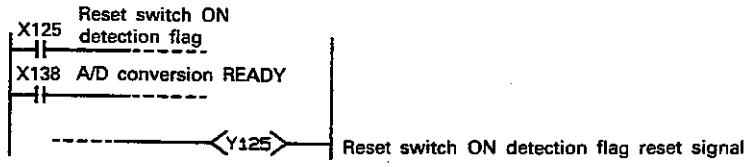
4.5.2 A68ADC control I/O signals automatic refresh setting

For details of contents of automatic refresh setting, refer to Section 3.6 MELSECNET/MINI(S3) Automatic Refresh of the A2A(S1)/A3ACPU User's Manual (Control Functions).
The following is an example of automatic refresh setting.



In the case of the system configuration and setting shown above, the A68ADC control I/O signals correspond to the device numbers shown below. Devices assigned to control input signals turn ON/OFF automatically as the A68ADC state changes.
When devices assigned to control output signals are turned ON/OFF by the sequence program, the device states are written to the batch refresh transmission areas of the master module and then transmitted to the A68ADC.

AnACPU device		A68ADC control I/O signal
X125 ←	X5	Reset switch ON detection flag
X138 ←	X18	A/D conversion READY
X125	→ Y5	Reset switch ON detection flag reset signal



4.6 Programming

This section describes the programming procedures when the MINI-S3 dedicated instructions of the AnACPU are used for data communication with the A68ADC connected to the MINI-S3 link.

4.6.1 Writing data to the A68ADC

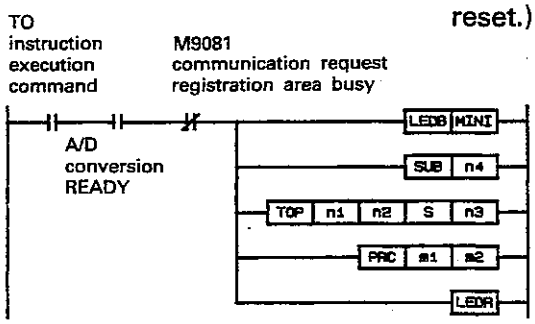
Instructions from LEDB MINI to LEDR are handled as one block of instructions in the sequence program to write data to the buffer memory of designated remote terminal module.
Items of the buffer memory and procedures of writing to the A68ADC are described below.

(a) Channel designation

(b) Averaging processing designation

(c) Averaging time and count designation by channel

(d) Error code clear ("0" is written from the AnACPU at error code reset.)



n1	Head station number of remote terminal module
n2	Head address of the buffer memory for writing
S	Head number of write data or of device which stores write data
n3	Number of write data
n4	Higher 2 digits of head I/O number assigned to AJ71PT32-S3
m1	Device number to be turned ON for 1 scan when execution of the TO instruction is completed
m2	Dummy device number

For details of instructions, refer to the A2A(S1)/A3ACPU Programming Manual (Dedicated Instructions).

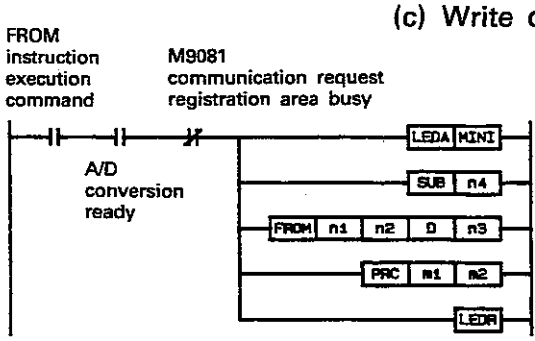
4.6.2 Reading data from the A68ADC

Instructions from LEDA MINI to LEDR are handled as one block of instructions in the sequence program to read data from the buffer memory of designated remote terminal module.
Items of the buffer memory and procedures of reading from the A68ADC are described below.

(a) Digital output of each channel

(b) A/D conversion completion flag

(c) Write data error code

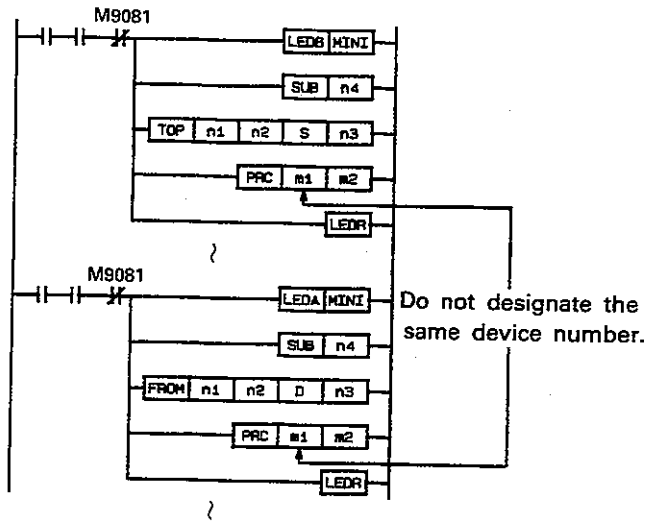


n1	Head station number of remote terminal module
n2	Head address of the buffer memory for reading
D	Head number of the device which stores read data
n3	Number of read data
n4	Head I/O number assigned to AJ71PT32-S3
m1	Device number to be turned ON for 1 scan when execution of the FROM instruction is completed
m2	Dummy device number

For details of instructions, refer to the A2A(S1)/A3ACPU Programming Manual (Dedicated Instructions).

4.6.3 Cautions on programming

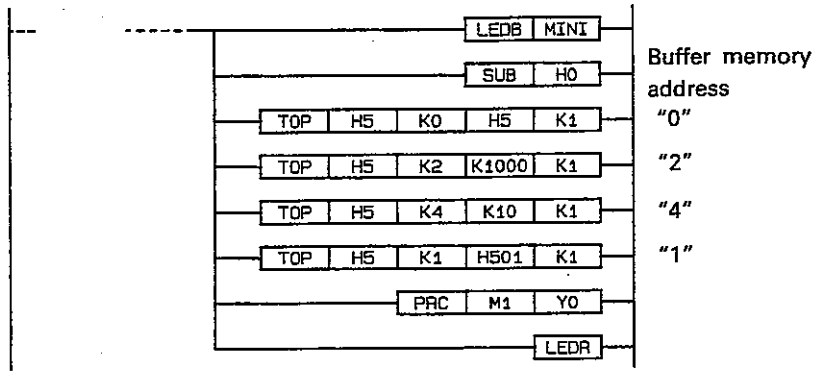
(1) It is necessary to provide the PRC instruction to the step immediately following the FROM/TO instruction. Use care not to designate same devices for "m1" of the PRC instruction and for "m1" of the PRC instruction provided to other step.



(2) The communication request registration areas can store a maximum of 32 FROM/TO instructions. If the 33rd FROM/TO instruction is executed, an operation error occurs.
Provide an interlock with M9081 and D9081 so that the FROM/TO instruction may not be executed when the communication request registration areas have become full.
M9081 and D9081 are described below.

Number	Contents	Details
M9081	OFF: Communication request registration area has a vacancy. ON: Communication request registration areas are full.	There are 32 communication request registration areas for remote terminals. Turns ON when all areas become full.
D9081	The number of vacant areas of the communication request registration area for remote terminals.	The number of vacant areas of the communication request registration area is stored.

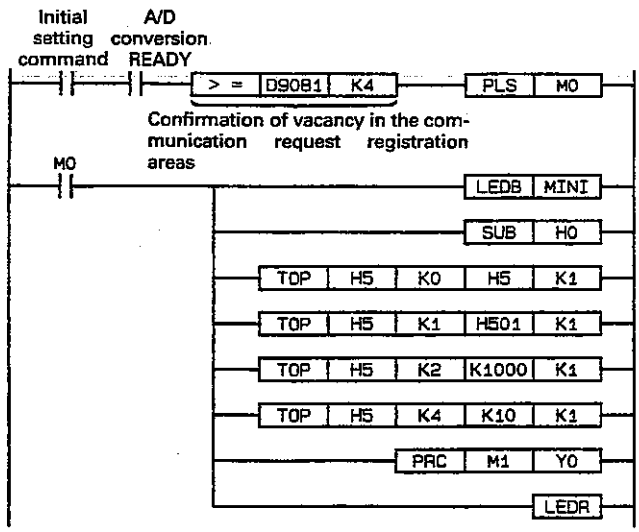
When data is written to two or more addresses in the buffer memory of the A68ADC, a single TO instruction can execute data write if the addresses are continuous. If the addresses are not continuous, it is necessary to execute the TO instruction at two or more points. (see below) In this case, the TO instruction information is stored in the communication request registration areas in plural.



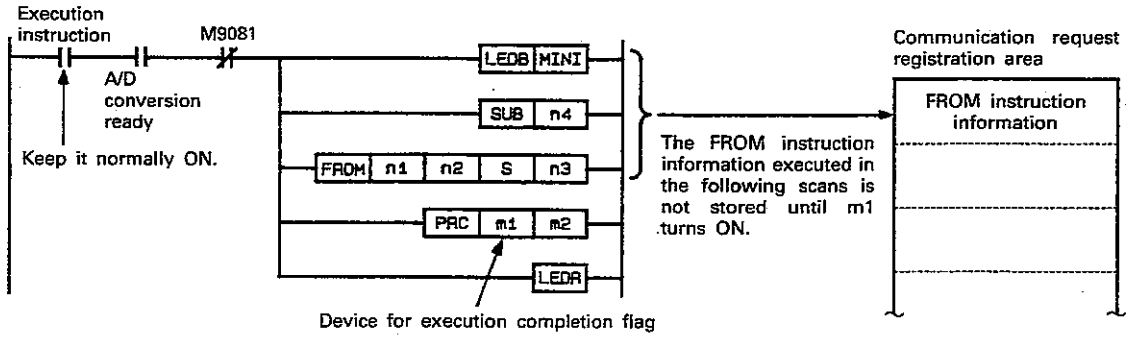
If an attempt is made to store the TO instruction information which is larger than the number of vacant areas of communication request registration areas, an error occurs and the CPU stops operation. To prevent this, it is necessary to provide a condition to allow confirmation that the vacancy in the communication request registration areas is larger than the number of TO instruction information. The programming example shown below describes the case when the TO instruction is executed after confirming the vacancy in the communication request registration areas.

Example) Initial setting program to the A68ADC

(Channel designation (buffer memory address 0) : Channels 1 and 3
Averaging processing of channel 1 (buffer memory address 2) : 1000 (ms)
Averaging processing of channel 3 (buffer memory address 4) : 10 (times)
Averaging processing designation (buffer memory addres 1))

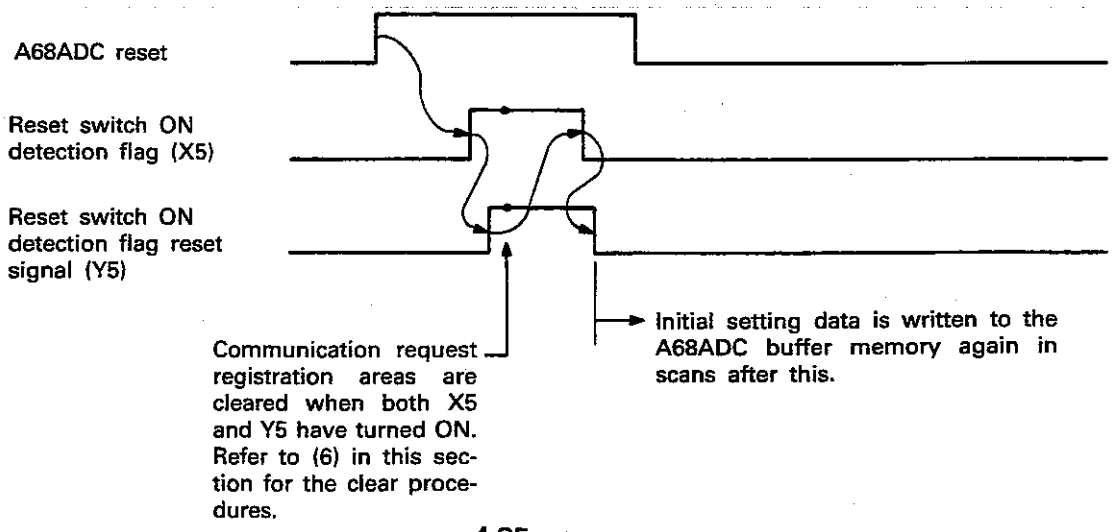


(3) Though the execution instruction of the FROM instruction is set to normally ON, the next FROM instruction information is not stored in the communication request registration areas until the processing of the FROM instruction being executed is completed and the execution completion flag designated by the PRC instruction turns ON. It is not necessary to provide an interlock to allow execution of the FROM instruction only after the execution completion flag has turned ON.

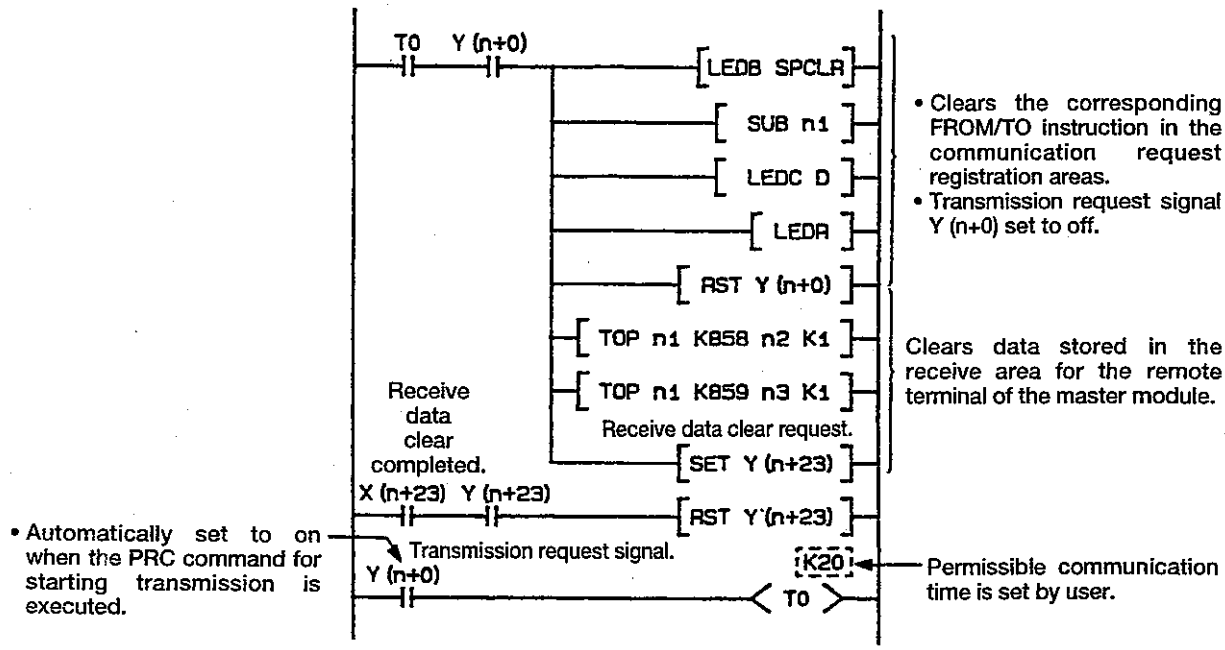


(4) For communication with the remote terminal modules linked to the AJ71PT32-S3, turn ON the AJ71PT32-S3 communication start signal Y(n+28) always before execution of each instruction. If the communication start signal has not turned ON, communication processings are not possible.
Though the MINI-S3 instruction is executed when the communication start signal is OFF, no error will occur. But, bit devices designated with m_1 of PRC m_1 m_2 does not turn ON.

(5) When the reset switch on the front of the A68ADC is moved to reset, the A68ADC returns to the initial state and performs D/A conversion with defaults.
Set the sequence program to continuously monitor the reset switch ON detection flag (X5) and, when the flag has turned ON, to clear the communication request registration areas and to write initial setting data again to the A68ADC. (when executed with other than defaults)



(6) If a communication completion response signal to the transmission executed to the A68ADC is not sent back, the CPU module is set in the state waiting for the communication completion signal infinitely unless the CPU module is reset. To prevent the infinite completion wait state, provide a monitoring timer to clear corresponding FROM/TO instruction information stored in the communication request registration areas when the timer has timed out.

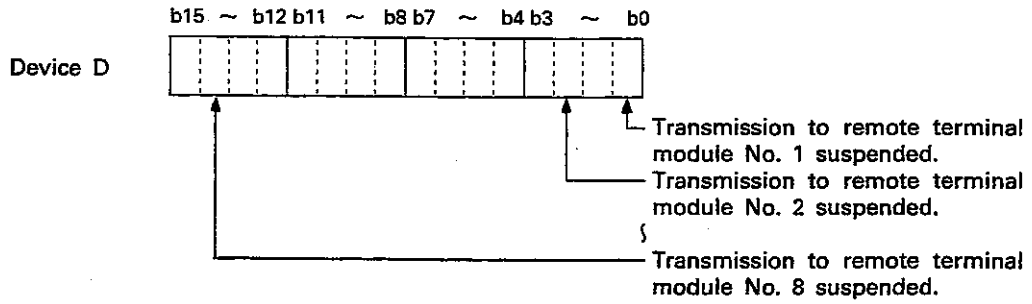


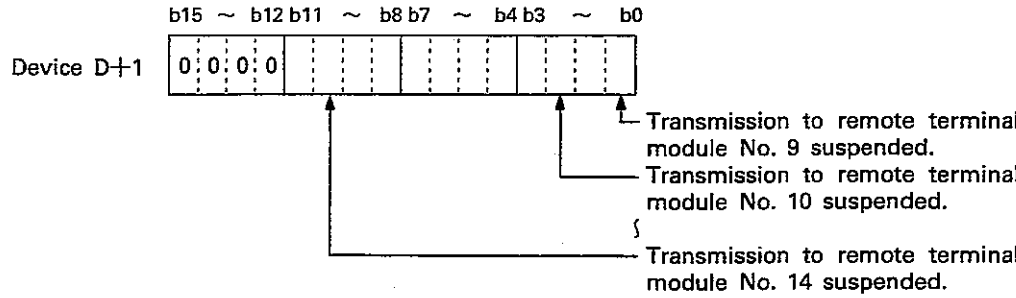
$X_{(n+23)}$, $Y_{(n+0)}$ and $Y_{(n+23)}$ are control I/O signals for the AJ71PT32-S3. See Section 4.3.2 for details.

Contents of n_1, n_2, n_3 and D designated by each instruction are as described below.

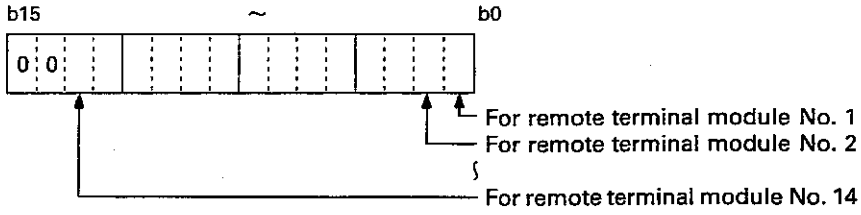
n_1: Higher 2 digits of head I/O number assigned to AJ35PT32-S3
Example) "12_H" when assigned to X/Y120 to 13F.

D : Data when the bit that corresponds to a processing to be suspended is set for "1".





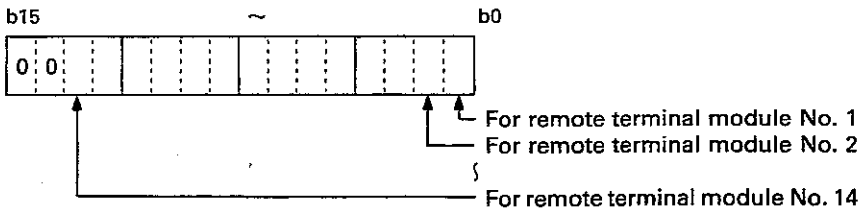
n_2: Receive buffer clear/no clear setting for each remote terminal number



0: No clear
1: Clear

Contents of setting are written to address 858 in the AJ71PT32-S3 buffer memory.

n_3: Clear execution range setting for each remote terminal number



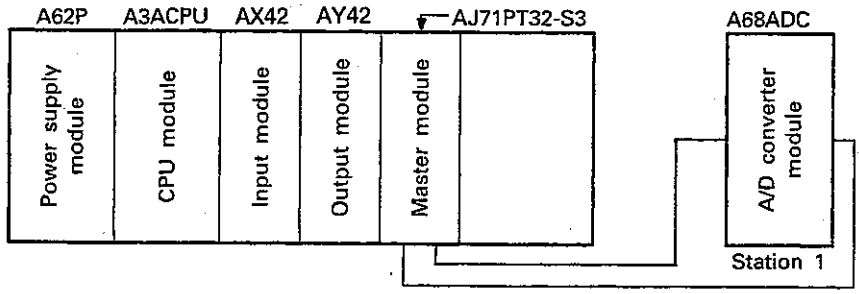
0: Only the remote terminal receive areas of the master module are cleared.
1: The remote terminal receive areas of the master module and the A68ADC receive buffer are cleared.

Contents of setting are written to address 859 in the AJ71PT32-S3 buffer memory.

(7) When automatic refresh is being set, the remote terminal module error detection $X_{(n+24)}$ of control I/O signals assigned to AJ71PT32-S3 turns ON for 1 scan after error detection.

4.6.4 Programming example

The following is a programming example when the digital output values of channels 1, 2 and 3 of the A68ADC are always read in the system configuration shown below.
Channel 1 is set for averaging by time (500 ms) and channel 2 is set for averaging by count (100 times). Channels 3 to 8 are not set for A/D conversion.



1) Contents of A3ACPU automatic refresh setting (See Section 4.5.2.)

Number of master modules: 1
Head I/O number: 80H
MINI/MINI-S3: MINI-S3
Receive data storage device: B000
Transmission data storage device: B100
Retry count: 7
FROM/TO response setting: Link priority
Faulty station data clear setting: Clear
Faulty station detection: D5000
Error No.: D6000
Total of remote I/O stations: 4
Transmission state setting at line error: 0

2) Contents of initial data ROM setting

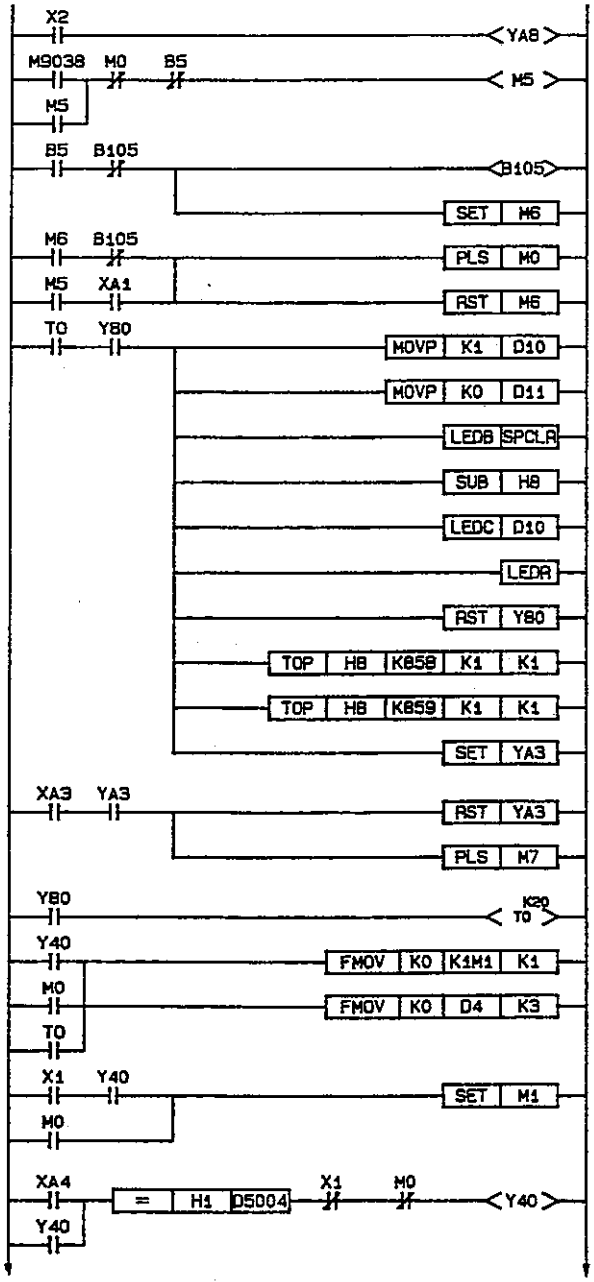
Total of linked stations: 4
Number of remote terminals: 1
Remote terminal No. 1: Station 1
Protocol: MINI standard
FROM address: 0
TO address: 500

3) I/O number of A68ADC control I/O signals when viewed from the PLC CPU (Automatic refresh setting)

Receive data storage device: B000 — B000 to B01F — X0 to X1F
Transmission data storage device: B100 ⇨
Total of remote I/O stations — B100 to B11F — Y0 to Y1F
: 4 stations → 32 points (8 points/station) — A68ADC I/O number viewed from CPU — A68ADC I/O number

4) Programming

- When X2 (MINI-S3 link communication start instruction) of the input module has turned ON, the MINI-S3 link starts.
- A/D conversion starts when the MINI-S3 link communicating signal has turned ON. When X0 (read start instruction) of the input module has turned ON, digital outputs are stored in D5 and D6.
- When an error is detected during communication with a remote terminal module, Y40 of the output module is turned ON to stop all processings.
  When X1 (communication error detection flag reset instruction) is turned ON, the error code storage areas and flags are all cleared.
- When the A68ADC is reset with the reset switch, all processings are stopped. When X2 (reset switch ON detection flag reset instruction) is turned ON, all flags are cleared.



Sets MINI-23 link communication start to on.

Resets the CPU unit or sets the M0 to on using a hardware reset from A68ADC and sets the reset switch on detection flag signal (B105) to on.

The process shown below is executed when the communication response monitoring time is exceeded.

(1) Clears the FROM, TO instruction data registered in the AnACPU communi cation request registration area.

(2) Sets Y80 to off (Transmission request signal to No.1 remote terminal module)

(3) Specifies clearing of receive signal area for the No. 1 remote terminal module of the master module and sets the receive signal data clear request signal (YA3).

M7 is set to on by the receive data clear completion (XA3) and resets the receive signal data clear request (YA3).

The communication response monitoring time is set by the user.

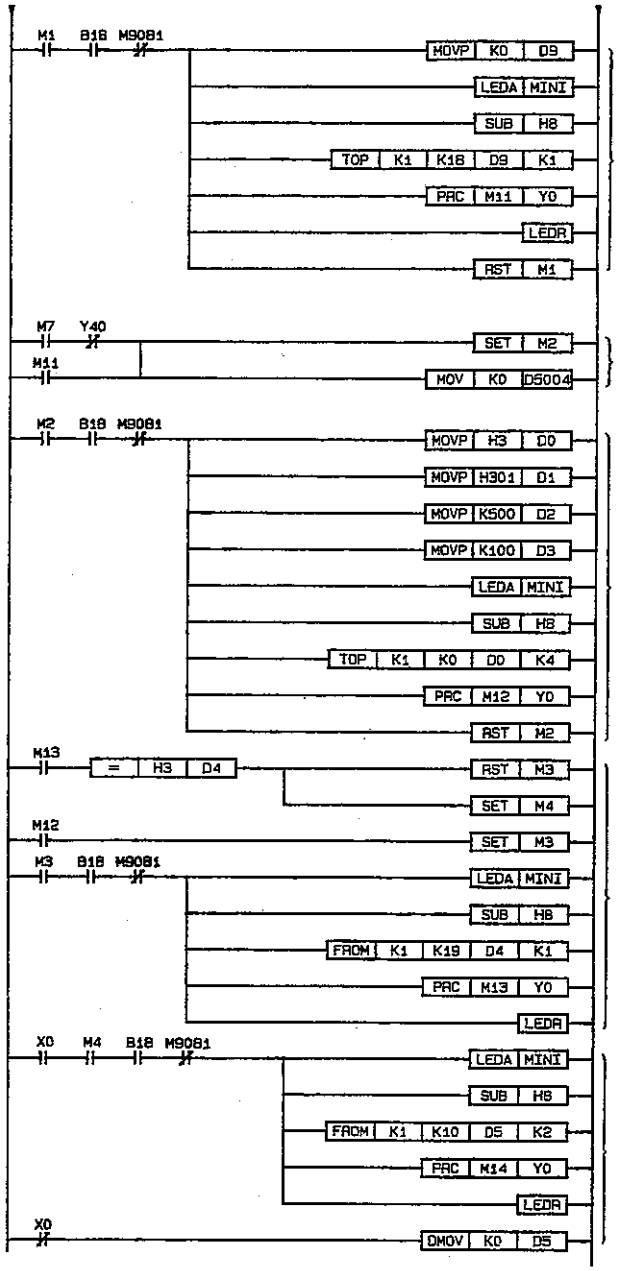
Clears M1 to M4, D4 to D6 when there is A68ADC main unit hardware reset operation, communication error, communication response monitoring timer over.

Set the error reset command (M1) for the A68ADC under the conditions shown below.

(1) Communication error reset command (X1).

(2) CPU reset or reset operation of the A68ADC main unit.

External display of No.1 remote terminal module error.



"0" is written to address 18 of buffer memory to clear A68ADC error code by the A68ADC error reset instruction (M1).

The A68ADC initial setting instruction (M2) is set on the conditions below.
(1) Remote terminal No. 1 receive data clear completion signal
(2) A68ADC error code clear completion

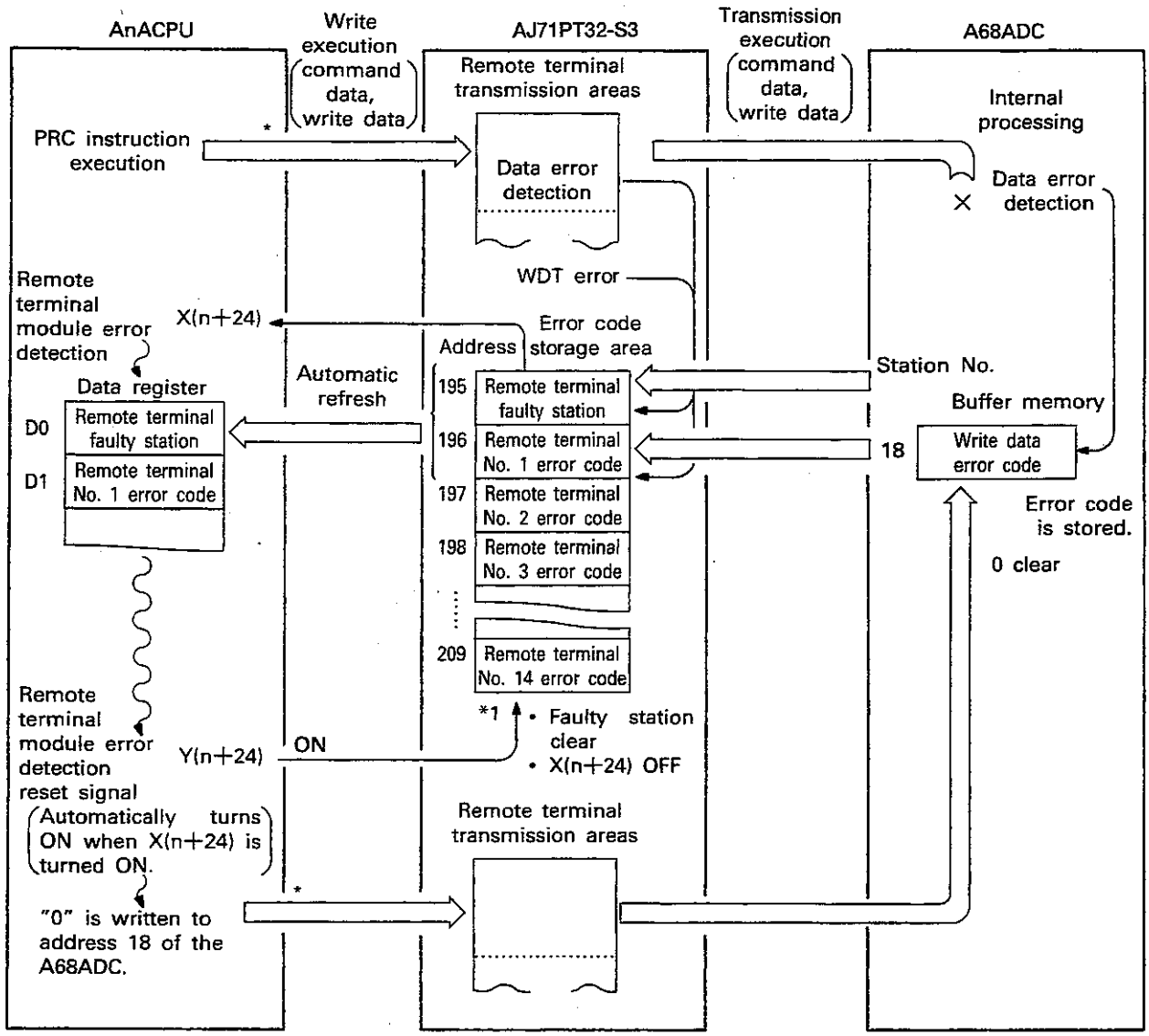
Data is stored in D0 to D3 and written to addresses 0 to 3 of A68ADC buffer memory by the A68ADC initial setting instruction.
D0: CH1 and CH2 are used.
D1:CH1 is set for averaging by time.
CH2 is set for averaging by count.
D2: CH1=500 ms } Averaging pro-
D3: CH2=100 counts } cessing

After writing initial setting data to the A68ADC, the A/D conversion completion flag is read from address 19 of the buffer memory.
When A/D conversion is completed (3H) on both CH1 and CH2, A/D conversion completion flag read is stopped and digital output read permission (M3) is turned ON.

When the digital output read instruction (X0) has turned ON, digital output values of CH1 and CH2 are read to D5 and D6.

4.7 Error Detection

The figure below shows the detecting procedure when errors have occurred when the AnACPU, A68ADC and AJ71PT32-S3 are used together.



Processings marked * by an asterisk are executed by the sequence program.

- When the remote terminal module error detection signal $X_{(n+24)}$ is turned ON, the AnACPU clears the FROM/TO instruction information for the corresponding remote terminal stored in the communication request registration areas, turns OFF the transmission request signal $Y_{(n+0)}$, and then, turns ON the remote terminal module error detection reset signal $Y_{(n+24)}$ for 1 scan.

5. LINKING TO THE ACPU AND THE AJ71PT32-S3

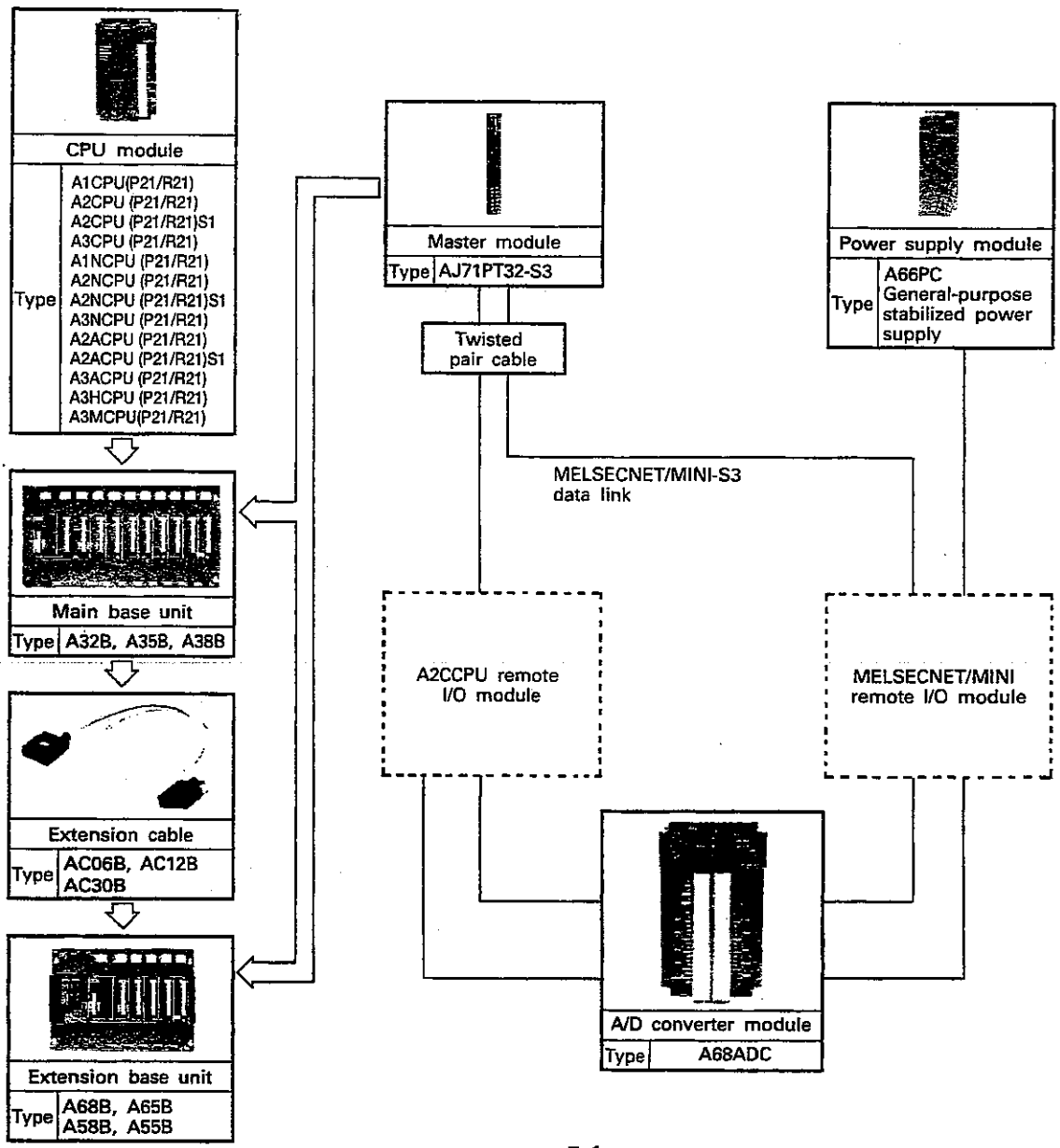
This section gives the linking procedures when an ACPU and AJ71PT32-S3 are used together and linked with the A68ADC on the MINI-S3 link.
The linking procedures when the MINI-S3 dedicated instructions are not used for the programs for the AnACPU in a system configuration which employs the combination of an AnACPU with the AJ71PT32-S3 are the same as those explained herein.

5.1 System Configuration

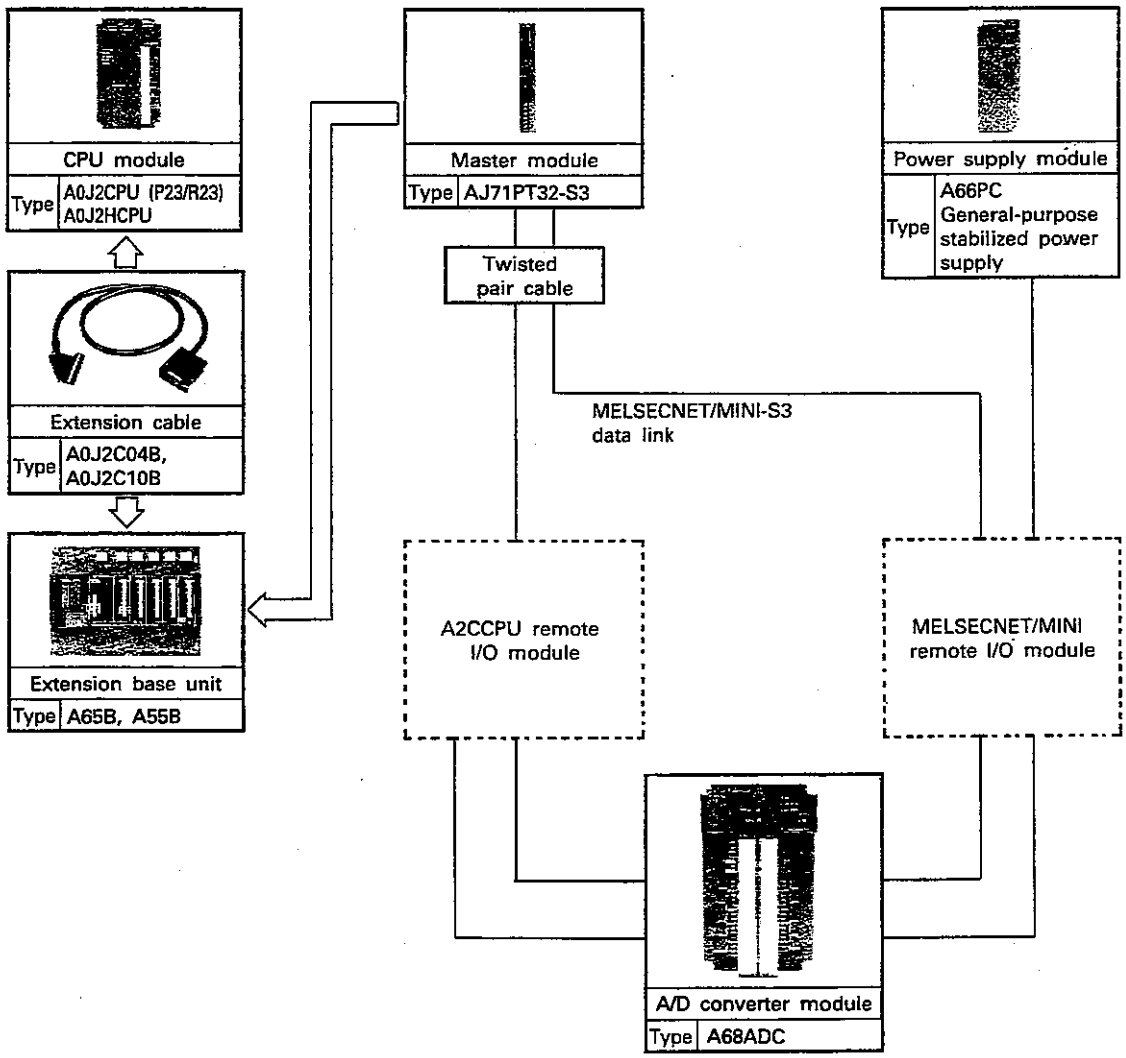
The following diagram shows the system configuration when the A68ADC is used as a remote terminal module of the MELSECNET/MINI-S3 with the AJ71PT32-S3 master module linked to the building block type CPU or the compact type CPU.

5.1.1 Overall configuration

(1) When the building block type CPU is used:



(2) When the compact type CPU is used:



5.1.2 Applicable system modules

The A68ADC can be used as a remote terminal module of the MELSECNET/MINI-S3 link with the AJ71PT32-S3 as its master module.

(1) A maximum of 14 remote terminal modules such as the A68ADC can be connected to an AJ71PT32-S3 module. The following types of modules are used as remote terminal modules.
- A68ADC (analog/digital converter module)
- AD61C (high speed counter module)
- A64DAVC (digital/analog voltage converter module)
- A64DAIC (digital/analog current converter module)
- AJ35PTF-R2 (RS232C interface module)
- AJ35PT-OPB-MI (mounting type operation box)
- AJ35T-OPB-PI (portable type operation box)

(2) Remote modules connected to the AJ71PT32-S3 can occupy up to 64 stations.

(3) The AJ71PT32-S3 can be connected to an independent CPU system or to the master station or a local station of the MELSECNET data link system. It cannot be connected to a remote I/O station.
The number of modules connected to one CPU module is not limited.

REMARK

For details of the MELSECNET/MINI-S3 link system, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

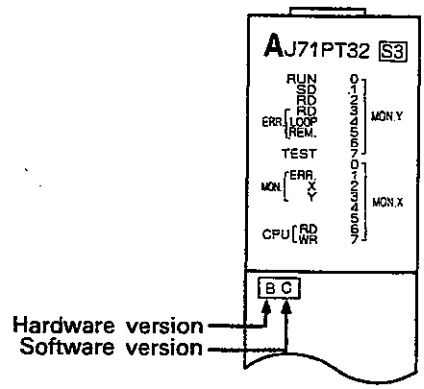
5.1.3 Cautions on constructing the system

(1) Twisted pair cables are used for connection between the AJ71PT32-S3 (master module) and the A68ADC.
The maximum connecting distance between stations varies with cable size when twisted pair cables are used.

0.2 mm^2 to smaller than 0.5 mm^2 ····· 50 m
0.5 mm^2 and larger ····· 100 m

(2) The A68ADC requires external supply of 24 VDC power for internal power supply. Use the A66PC power supply module or a general-purpose stabilized power supply (24 VDC). If one power supply is connected to two or more A68ADC or remote I/O modules, select proper cables and wiring route considering voltage drop due to cables.
Refer to Section 3.1.2 (3) for calculation of voltage drop.

(3) The AJ71PT32-S3 (master module) that can use A68ADC is one that has software version "C" or later shown on the front of the module
Note that software versions "A", "B" are shown on the front of the master module, or when no version is shown, the AJ71P7_32-S3 cannot be used.



(4) AJ71PT32-S3 cannot be installed to the last slot of 7th extension stage of the A3CPU (P21/R21)

IMPORTANT

Use the AJ71PT32-S3 (master module) in the extension mode (48 occupied points). Be sure to mount the initial data ROM storing the total number of remote stations and remote terminal data (set station numbers of remote terminal modules and corresponding remote terminal numbers) to the master module.

5.2 Data Communication Processings

5.2.1 Communication processes

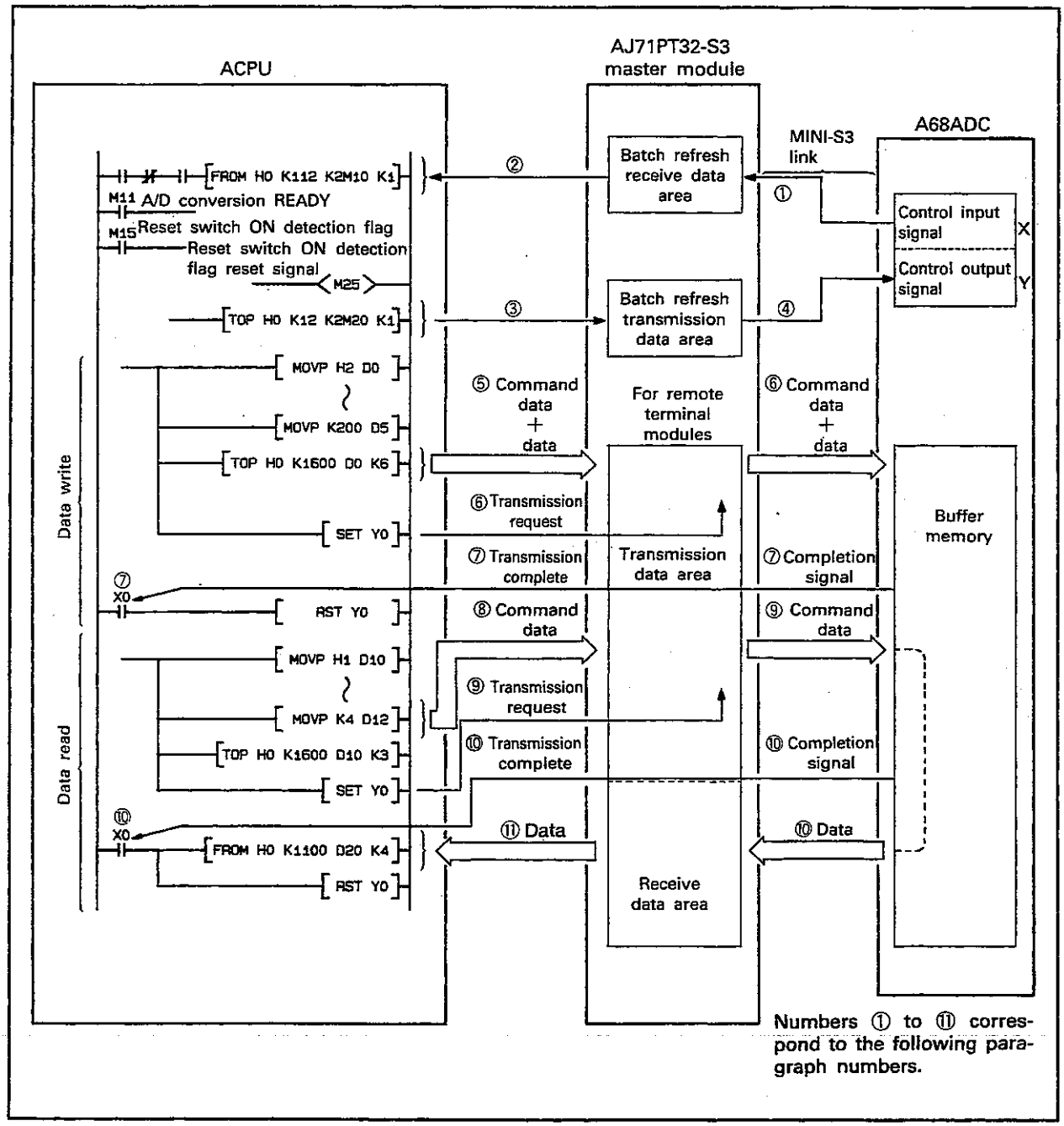


Fig. 5.1 Communication Procedures

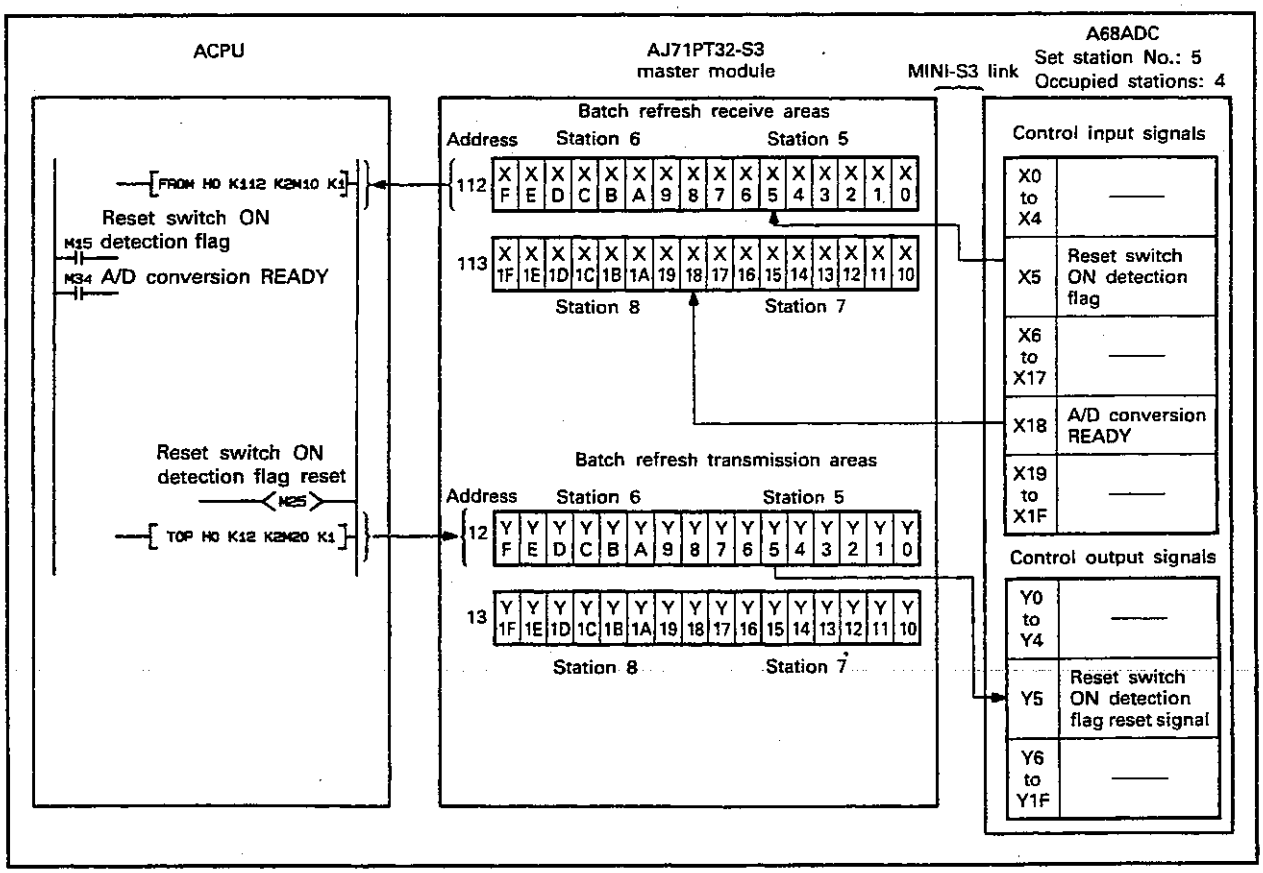
(1) Communication processes of control input/output signals used for interlocking of the A68ADC and the ACPU

① Control input signals from the A68ADC are stored automatically in the batch refresh receive data area in the master module at 3.5 to 18 msec intervals.

② Control input signals stored in the batch refresh receive data area are read to designated devices by the FROM instruction.

③ By designating the devices that correspond to the control signals output to the A68ADC with the TO instruction, state data of the designated devices are stored in the batch refresh transmission data area.

④ Control output signals stored in the batch refresh transmission data area are transmitted to the A68ADC at 3.5 to 18 msec intervals.



(2) Writing data to the A68ADC buffer memory

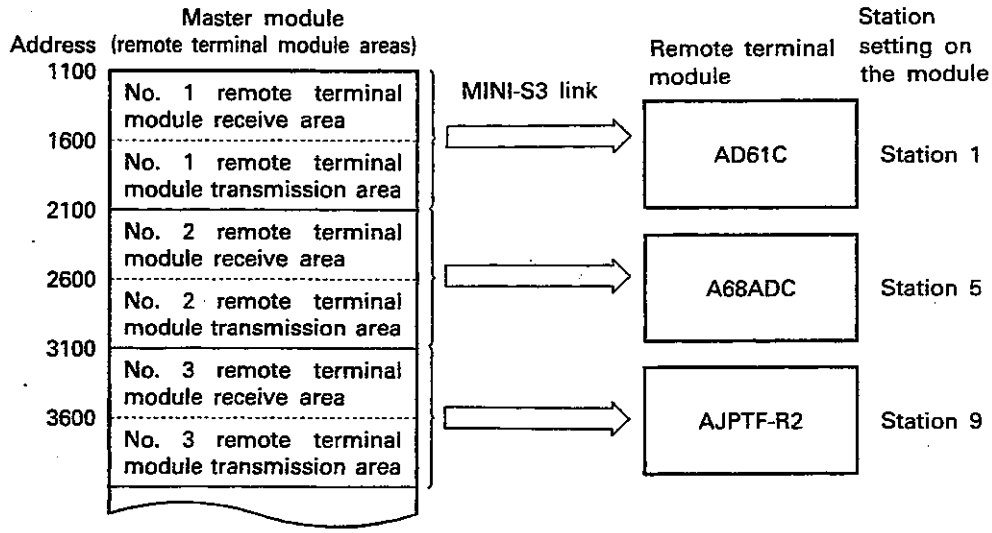
⑤ Command data and write data such as the write execution command to the A68ADC are stored in the remote terminal transmission data area by the TO instruction.

⑥ By execution of the SET $Y_{(n+0)}$ instruction, command data and write data stored in the remote terminal transmission data area are transmitted to the A68ADC.
Transmission data is sent in several times of communication.
The remote terminal module areas correspond to the remote terminal modules connected to the MINI-S3 link as shown below.

When the initial data stored in the initial data ROM mounted to the master module is as shown right:

No. 1 remote terminal = Station 1
No. 2 remote terminal = Station 5
No. 3 remote terminal = Station 9

See Section 5.5.1 for details of the initial data.



⑦ When data is written to the A68ADC buffer memory and internal processing is completed, the completion signal is sent back to the master module.
When the master module has received the completion signal, the transmission completion signal $X_{(n+0)}$ is turned ON.

(3) Reading data from the A68ADC buffer memory

⑧ Command data such as the read execution command from the A68ADC is stored in the remote terminal transmission data area by the TO instruction.

⑨ By execution of the SET $Y_{(n+0)}$ instruction, command data stored in the remote terminal transmission data area is sent to the A68ADC.
Transmission data is sent in several times of communication.

⑩ When the A68ADC has received the command data and after internal processing is completed, the read data is transmitted to the remote terminal receive data area of the master module and the completion signal is sent back.
When the master module has received the completion signal, the transmission completion signal $X_{(n+0)}$ is turned ON.
For details of the transmission completion signal, refer to Section 5.3.2 "Input signals of AJ71PT32-S3".

⑪ After confirming that the transmission completion signal is turned ON, read data stored in the remote terminal receive data area of the master module is read by the FROM instruction.

5.2.2 Processing time

This section introduces the processing time up to the writing of the A68ADC buffer memory data and processing time up to the reading of the data from the buffer memory.

(1) Processing time when writing data.

Maximum processing time
= 3 scan time *1 + tms × (number of write data words + 8)
+40ms *2

(2) Processing time when reading data

Maximum processing time
= 3 scan time *1 + tms × (number of read data words +9)
+40ms *2

*1: The usage time for dedicated commands or partial refresh is 3 --> 1.
*2: A68ADC internal processing time.

"t" is the I/O refresh time and varies with the number and type of connected remote module stations.
The I/O refresh time is calculated as follows.

Mode	Mode Setting	I/O Refresh Time (msec)
Extension mode (48 points)	Automatic return enable (0)	t = 0.66 + (0.044 × R) + (0.25 × B) + (0.95 × T)
	Automatic return disable (1)	t = 0.54 + (0.058 × R) + (0.25 × B) + (0.95 × T)
	Communication stop at error detection (2)	t = 0.54 + (0.051 × R) + (0.25 × B) + (0.95 × T)

R : Total number of remote stations
B : Number of AJ35PTF-128DT modules
T : Number of remote terminal modules

5.3 Input/output Signals Handled With the PC CPU

5.3.1 I/O signals of the A68ADC

Functions of the control input and output signals handled between the A68ADC and ACPU are described in this section. Devices X refer to the input signals from the A68ADC to the ACPU. Devices Y refer to the output signals from the ACPU to the A68ADC.

Signal Direction: A68ADC → ACPU		Signal Direction: ACPU → A68ADC	
Device No.	Description	Device No.	Description
X0 to X4	Unusable	Y0 to Y4	Unusable
X5	Reset switch ON detection flag of the A68ADC module		
X6 to X17	Unusable		
X18	A/D conversion ready (1) Turns ON when A/D conversion is ready in the normal mode (other than the test mode) after the power was turned on or the PC CPU was reset. Turns OFF when mode is switched from normal to test. (2) Used for the interlock for reading and writing from the PC CPU to the A68ADC.		
		Y5	Reset switch ON detection flag reset signal
X19 to X1F	Unusable	Y6 to Y1F	Unusable

Table 4.1 List of Input/output Signals

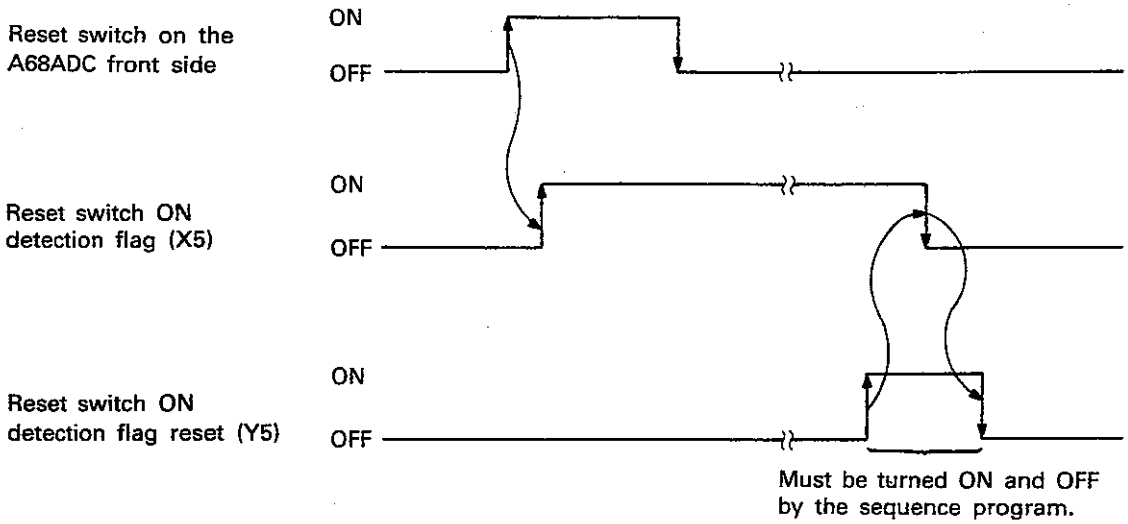
REMARK

A/D conversion ready is established when digital output data is stored in the buffer memory after one time of completion of A/D conversion on all of 8 channels.

IMPORTANT

Devices Y0 to Y4, and Y6 to Y1F are unusable since they are used in the system.
If any of these devices are used (ON/OFF) in the sequence program, functions of the A68ADC are not guaranteed.

(1) Reset switch ON detection flag (X5) and reset switch ON detection flag reset signal (Y5)
Turns ON (latched) when the reset switch of the A68ADC is moved to reset.
To restart communication, turn ON the reset switch ON detection flag reset signal (Y5) with the sequence program.



POINT

(1) If the A68ADC is reset by moving the reset switch, it returns to the initial state. Start operation from the initial setting.
(2) Since X5 turns ON also after the power is turned on, be sure to turn ON Y5 and OFF X5 at the initial stage. And then, execute program for the A68ADC.

5.3.2 I/O signals of the AJ71PT32-S3

Device No.	Signal Name		Device No.	Signal Name	
X (n+0)	Transmission completion signal	For remote terminal module No. 1	Y (n+0)	Transmission request signal	For remote terminal module No. 1
X (n+1)	Read request signal		Y (n+1)	Read completion signal	
X (n+2)	Transmission completion signal	For remote terminal module No. 2	Y (n+2)	Transmission request signal	For remote terminal module No. 2
X (n+3)	Read request signal		Y (n+3)	Read completion signal	
X (n+4)	Transmission completion signal	For remote terminal module No. 3	Y (n+4)	Transmission request signal	For remote terminal module No. 3
X (n+5)	Read request signal		Y (n+5)	Read completion signal	
X (n+6)	Transmission completion signal	For remote terminal module No. 4	Y (n+6)	Transmission request signal	For remote terminal module No. 4
X (n+7)	Read request signal		Y (n+7)	Read completion signal	
X (n+8)	Transmission completion signal	For remote terminal module No. 5	Y (n+8)	Transmission request signal	For remote terminal module No. 5
X (n+9)	Read request signal		Y (n+9)	Read completion signal	
X (n+A)	Transmission completion signal	For remote terminal module No. 6	Y (n+A)	Transmission request signal	For remote terminal module No. 6
X (n+B)	Read request signal		Y (n+B)	Read completion signal	
X (n+C)	Transmission completion signal	For remote terminal module No. 7	Y (n+C)	Transmission request signal	For remote terminal module No. 7
X (n+D)	Read request signal		Y (n+D)	Read completion signal	
X (n+E)	Transmission completion signal	For remote terminal module No. 8	Y (n+E)	Transmission request signal	For remote terminal module No. 8
X (n+F)	Read request signal		Y (n+F)	Read completion signal	
X (n+10)	Transmission completion signal	For remote terminal module No. 9	Y (n+10)	Transmission request signal	For remote terminal module No. 9
X (n+11)	Read request signal		Y (n+11)	Read completion signal	
X (n+12)	Transmission completion signal	For remote terminal module No. 10	Y (n+12)	Transmission request signal	For remote terminal module No. 10
X (n+13)	Read request signal		Y (n+13)	Read completion signal	
X (n+14)	Transmission completion signal	For remote terminal module No. 11	Y (n+14)	Transmission request signal	For remote terminal module No. 11
X (n+15)	Read request signal		Y (n+15)	Read completion signal	
X (n+16)	Transmission completion signal	For remote terminal module No. 12	Y (n+16)	Transmission request signal	For remote terminal module No. 12
X (n+17)	Read request signal		Y (n+17)	Read completion signal	
X (n+18)	Transmission completion signal	For remote terminal module No. 13	Y (n+18)	Transmission request signal	For remote terminal module No. 13
X (n+19)	Read request signal		Y (n+19)	Read completion signal	
X (n+1A)	Transmission completion signal	For remote terminal module No. 14	Y (n+1A)	Transmission request signal	For remote terminal module No. 14
X (n+1B)	Read request signal		Y (n+1B)	Read completion signal	
X (n+1C)	Unusable		Y (n+1C)	Unusable	
X (n+1D)			Y (n+1D)		
X (n+1E)			Y (n+1E)		
X (n+1F)			Y (n+1F)		
X (n+20)	Hardware error		Y (n+20)		
X (n+21)	MINI-S3 link communicating		Y (n+21)		
X (n+22)	Unusable		Y (n+22)		
X (n+23)	Receive data clear completion		Y (n+23)	Receive data clear request	
X (n+24)	Remote terminal module error detection		Y (n+24)	Remote terminal module error detection reset	
X (n+25)	Test mode		Y (n+25)	Unusable	
X (n+26)	MINI-S3 link error detection		Y (n+26)		
X (n+27)	MINI-S3 link communication error		Y (n+27)		
X (n+28)	ROM error		Y (n+28)	MINI-S3 link communication start	
X (n+29)	Unusable		Y (n+29)	Unusable	
X (n+2A)			Y (n+2A)	FROM/TO instruction response designation	
X (n+2B)			Y (n+2B)	Faulty station data clear designation	
X (n+2C)			Y (n+2C)	Switching the buffer memory channel.	
X (n+2D)			Y (n+2D)	Error reset	
X (n+2E)			Y (n+2E)	Unusable	
X (n+2F)			Y (n+2F)		

Table 5.2 List of I/O Signals

"n" specifies value of the head I/O address of the AJ71PT32-S3.
Example) When the I/O address of the AJ71PT32-S3 is between X/Y20 and X/Y4F: X (n + 0) to X (n + 2F) = X20 to X4F
Y (n + 0) to Y (n + 2F) = Y20 to Y4F

REMARK

For details of functions and purposes of control I/O signals, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

5.4 Assignment of Buffer Memory

5.4.1 Contents and configuration of the A68ADC buffer memory

Assignment of the A68ADC buffer memory (without battery backup) is shown below.

Address (Decimal)		
0	Number of channels	Read and write from CPU
1	Averaging processing specification	
2	CH1 averaging time, count	
3	CH2 averaging time, count	
4	CH3 averaging time, count	
5	CH4 averaging time, count	
6	CH5 averaging time, count	
7	CH6 averaging time, count	
8	CH7 averaging time, count	
9	CH8 averaging time, count	
10	CH1 digital output value	Read from CPU
11	CH2 digital output value	
12	CH3 digital output value	
13	CH4 digital output value	
14	CH5 digital output value	
15	CH6 digital output value	
16	CH7 digital output value	
17	CH8 digital output value	
18	Write data error code	Read and write from CPU
19	A/D conversion completion flag	Read from CPU

*All 16-bit data.

POINT

Addresses 10 to 17 and 19 of the buffer memory are areas exclusively used for reading from the PLC CPU. Because the A68ADC overwrites digital data in these areas always destroying the buffer memory data. In this case, the A68ADC detects an error, stores the error code in address 18 and flickers the RUN LED.

(1) Channel designation (Address 0)

(a) At power on, channel designation is set at "00FF$_H$ (255)" for A/D conversion on all channels.

(b) In order to reduce sampling time, channel designation can be changed by the sequence program.

(c) For channel designation change, A/D conversion must be set by each channel.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
–	–	–	–	–	–	–	–	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Ignored

Channel designation
1: A/D conversion enable
0: A/D conversion disable

Default is "1" for all channels.

(Example) To designate channels 1 and 3 and 4 for A/D conversion.
By writing 000D$_H$ (13) to designate channels for A/D conversion, sampling time is obtained as 2.5 ms × 3 = 7.5 ms.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	→ 000D$_H$ (13)
								CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	

(2) Averaging processing designation (Address 1)

(a) When the power is turned on and the A/D conversion READY signal of A68ADC is on, all channels are set to sampling processing.

(b) For selection of sampling processing or averaging processing use address 1 of the buffer memory.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Specification of channel for which averaging processing will be performed
1: Averaging processing
0: Sampling processing

Specification of time/count
1: Time averaging
0: Count averaging

POINT

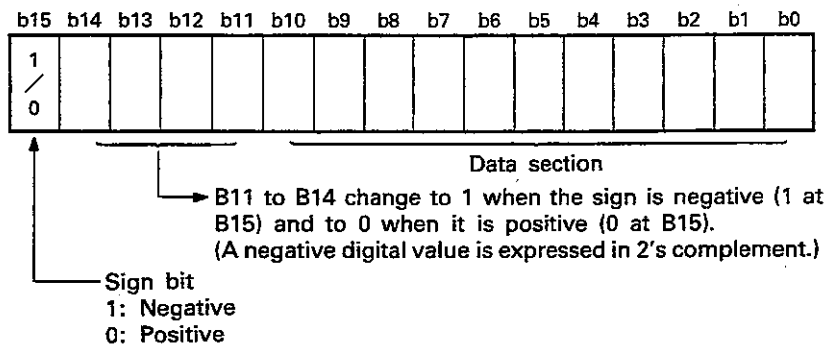
When averaging processing is not specified, sampling processing is set without regard to the specification of time/count.

(3) Averaging time, averaging count (Addresses 2 to 9)
a) At power-on, the averaging time and averaging count are set to 0.
b) The setting ranges are as indicated below:
Averaging processing in terms of count: 1 to 4000 times
Averaging processing in terms of time: 20 to 10000 ms

POINT

If a value outside the above range has been written, setting error occurs and the buffer memory is rewritten. However, the A68ADC performs A/D conversion processing at the averaging time or count previously set.

(4) Digital output value (Addresses 10 to 17)
The digital output value is expressed in 16-bit, signed binary within the range from −2048 to +2047.



(5) Write data error code (Address 18)
a) When data is read from the PLC CPU, the A68ADC makes a data range check for the number of channels, averaging count and averaging time and also performs read/write area access check only once. If any value is outside the range, the A68ADC stores the error code in 16-bit binary. For details of error codes, see Section 7.1.
b) To reset an error code, write 0 from the programmable controller CPU.
c) When several error codes have occurred, the data error code, which has been detected by the A68ADC first, is stored. The other errors are not stored.
d) If an error is reset without remedying the error, the data error code is set to 0 and the RUN LED of A68ADC stops flickering.

(6) A/D conversion completion flag (Address 19)

(a) The A/D conversion completion flag is set to 1 when the A/D conversion ready signal (X1) is turned ON after power on.
When the A/D conversion ready signal has turned ON, A/D conversion on all of 1 to 8 channels is completed, and $00FF_H$ (255) is stored in the buffer memory.

(b) The A/D conversion completion flag processing after power on is performed only once when channel designation for A/D conversion (address 0) is changed.

- Channel designation change from 0 to 1:
  (If averaging processing has been designated, averaging processing of averaging count or time is completed, and then, the A/D conversion digital values are stored in the buffer memory. And, the flag is set to 1.)
- Channel designation change from 1 to 0:
  The A/D conversion completion flag of corresponding channel is set to 0.

(c) The A/D conversion completion flag is provided to each channel.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

Channel designation
1: A/D conversion completed.
0: A/D conversion not completed.

(d) The A/D conversion completion flag can be used for the interlock when reading the digital value of the channel for which averaging processing is executed.

5.4.2 Contents and configuration of the AJ71PT32-S3 buffer memory

The AJ71PT32-S3 is provided with a buffer memory (without battery backup) for data communication with the PLC CPU.
Use the FROM/TO instructions to read and write data from to the buffer memory.

(1) Assignment of the buffer memory

Address (decimal)		Content	Read/write by PLC CPU
0	(Unused)	—	Read/write enable
1	Retry count	Sets the number of retries when communication error has occurred.	
	(Unused)	—	
4	Line error check	Checks location of line error.	
	(Unused)	—	
10 to 41	Batch refresh transmission data	Writes data to be output to the batch refresh type remote I/O module.	
	(Unused)	—	—
70 to 77	Remote module card information	Stores type identification of each remote module being connected.	Read only
	(Unused)	—	—
90 to 93	Accumulated faulty station detection	Stores faulty remote station numbers. (Detected state is retained until reset.)	Read/write enable
	(Unused)	—	—
100 to 103	Faulty station detection	Stores faulty remote station numbers. (Update state is retained.)	Read only
	(Unused)	—	
107	Communication error code	Stores the cause of the MINI-S3 link communication error signal ON.	
108	Error detection code	Stores accumulated count of the MINI-S3 link error detection ON.	
	(Unused)	—	
110 to 141	Batch refresh receive data	Stores the input data from the batch refresh type remote I/O modules.	
	(Unused)	—	
160	Line error retry counter	Stores the number of retries when communication with all remote modules fails due to line error.	
161 to 192	Retry counter	Stores the number of retries executed to faulty stations.	
	(Unused)	—	
195	Remote terminal module faulty station	Stores the station number when a remote terminal module has caused an error.	
196 to 209	Remote terminal module error code	Stores the cause of the remote terminal module error detection signal X(n+24) ON.	
	(Unused)	—	—
250 to 282	Partial refresh station set data	Writes the station number and digit designation (number of time of division) of the partial refresh type remote I/O module.	Read/write enable
	(Unused)	—	
300 to 363	Partial refresh transmission data	Writes data to be output to the partial refresh type remote I/O module.	
	(Unused)	—	
598	Partial refresh accumulated input error detection	Stores the input faulty station number of the partial refresh type remote I/O module input data. (Detected state is retained until reset.)	
599	Partial refresh input error detection	Stores the input faulty station number of the partial refresh type remote I/O module input data. (Update state of communication is stored.)	
600 to 663	Partial refresh receive data	Stores input data of the partial refresh type remote I/O module.	Read only

Address (decimal)			Content	Read/write by PLC CPU
858	Receive data clear designation		Sets the AJ35PTF-R2 station that clears receive data by the receive data clear request signal Y(n+23).	Read/write enable
859	Receive data clear range designation		Designates the receive buffer that clears receive data by the receive data clear request signal Y(n+23).	
860 to 929	No-protocol mode parameter		Sets the parameters when the AJ35PTF-R2 is used in the no-protocol mode.	
930 to 1099	(Unused)		—	—
	(*1) Channel 0	(*1) Channel 1		
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8	Areas to which transmission data to remote terminal modules is written or to store data received from remote terminal modules.	Read/write enable
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9		
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10		
4100 to 5099	Communication area for remote terminal No. 4	Communication area for remote terminal No. 11		
5100 to 6099	Communication area for remote terminal No. 5	Communication area for remote terminal No. 12		
6100 to 7099	Communication area for remote terminal No. 6	Communication area for remote terminal No. 13		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14		
	$Y_{(n+2C)}$: OFF	$Y_{(n+2C)}$: ON		

POINT

(1) Channels specified with *1 are used for read/write in areas of addresses 1100 to 8099 and are switched by the channel switching signal $Y_{(n+2C)}$.

(2) The buffer memory is all cleard (0 is stored.) at power on or when the PLC CPU is reset. However, retry count (adress 1) and no-protocol mode parameters (addresses 860 to 929) are set at defaults.

(3) Do not write data from the PLC CPU to read only areas.

(4) Unused areas are used by the system of the master module.

(5) Data in the buffer memory can be read continuously including unused areas. For example, data of accumulated faulty stations detection (addresses 90 to 93) and faulty station detection (addresses 100 to 103) can be read by a single FROM instruction.

REMARK

For details of contents at each address and data configuration of the buffer memory, refer to AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual.

(2) Remote terminal communication areas (addresses 1100 to 8099)

(a) Areas for data communication with remote terminal modules.

(b) The communication areas are assigned to two channels. Channel 0 is assigned to remote terminal modules No. 1 to No. 7, and channel 1 is assigned to remote terminal modules No. 8 to No. 14.
If the FROM/TO instructions are used for data read/write, switch channels to the corresponding remote terminal modules.
Channel switching is performed by the channel switching signal $Y_{(n+2C)}$.

	Channel 0	Channel 1
1100 to 2099	Communication area for remote terminal No. 1	Communication area for remote terminal No. 8
2100 to 3099	Communication area for remote terminal No. 2	Communication area for remote terminal No. 9
3100 to 4099	Communication area for remote terminal No. 3	Communication area for remote terminal No. 10
4100		
7099		
7100 to 8099	Communication area for remote terminal No. 7	Communication area for remote terminal No. 14
	$Y_{(n+2C)}$: OFF	$Y_{(n+2C)}$: ON

The remote terminal module number refers to the number assigned to each remote terminal module set in the initial data ROM of the master module.
Data read/write is executed for areas which correspond to the module numbers assigned to each remote terminal module.

(c) Each communication area consists of a transmission area and a receive area. Capacity of each area at power on is 500 words.

	Communication area for remote terminal module No. 1
1100 to 1599	Receive area (FROM area)
1600 to 2099	Transmission area (TO area)

The transmission area sets data to be transmitted to remote terminal modules.
The receive area stores data received from remote terminal modules.

(d) Capacity of the transmission and receive areas can be changed by the initial data setting of the master module. (Note that the total capacity of the two areas must not exceed 1000 words.)
Example) Receive area: 200 words, Transmission area: 800 words

5.5 Contents of Initial Setting

The contents of initial setting when the A68ADC is used as a remote terminal module are described.

5.5.1 Initial setting of the AJ71PT32-S3

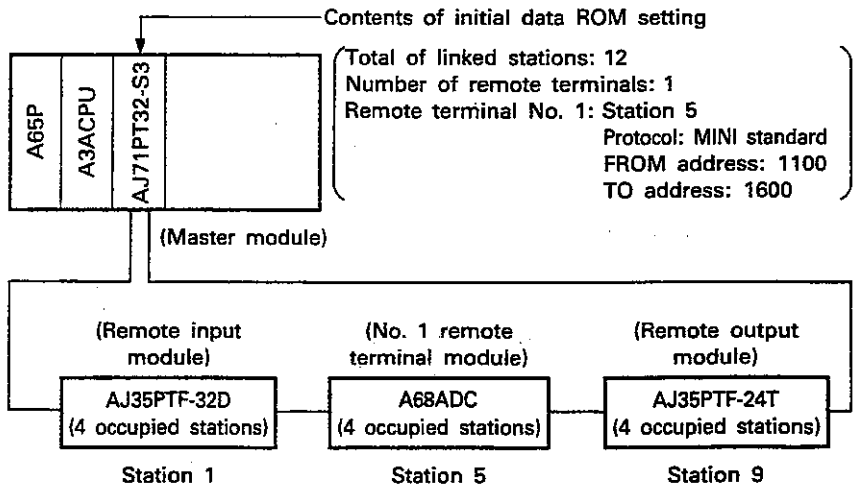
Use the SW□GP-MINIP system disk to set initial data and to store it in the initial data ROM.
The initial data ROM is inserted to the ROM socket of the AJ71PT32-S3.
Contents of initial data setting are mentioned below.

- Total number of remote stations: Set the total number of occupied stations of each module connected to the MINI-S3 link.
  Example) AJ35PTF-32A (remote I/O module) 4 stations
  A68ADC (remote terminal module) 4 stations
  AJ35PTF-24T (remote I/O module) 4 stations
  Total: 12 stations
- Station number of each remote terminal number: Set the station numbers set for modules which correspond to remote terminal modules No. 1 to No. 14.
  Example) AJ35PTF-32A 1 stations
  A68ADC 5 stations ← Remote terminal module
  AJ35PTF-24T 9 stations
  Remote terminal No. 1=5 stations
- Protocol: Set the protocol used for communications with the A68ADC.
  Use the MINI standard protocol.
- Remote terminal FROM/TO area setting:
  Set the capacity for the FROM area and the TO area as explained in Section 5.4.2 (2).
  Default is 500 words for each of the FROM area and the TO area.

For details of setting procedures, refer to SW□GP-MINIP Operating Manual.

5.6 Programming

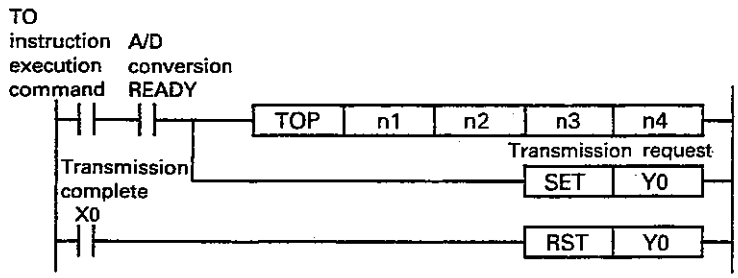
This section describes the programming procedures for writing setting data to the A68ADC and reading digital output values with a system configuration shown below.



5.6.1 Writing data to the A68ADC

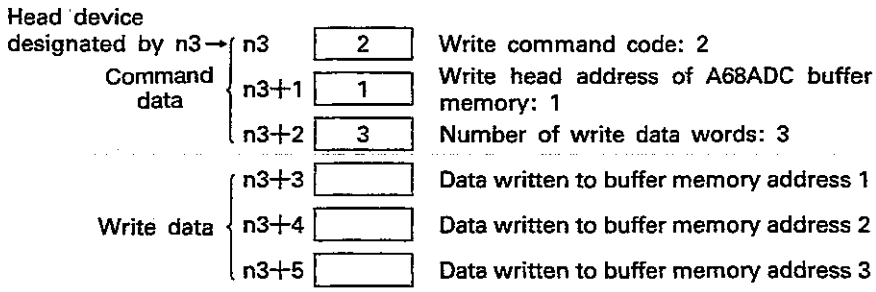
The TO instruction in the sequence program is used to write data to the buffer memory of designated remote terminal module. Items of the buffer memory and procedures of writing to the A68ADC are described below.

(a) Channel designation
(b) Averaging processing designation
(c) Averaging time and count designation by channel
(d) Error code clear ("0" is written from the ACPU at error code reset.)



n1	Head I/O number assigned to AJ71PT32-S3
n2	Head address of the remote terminal transmission areas
n3	Head device number of data register which stores command data.
n4	Total number of words of command data and write data

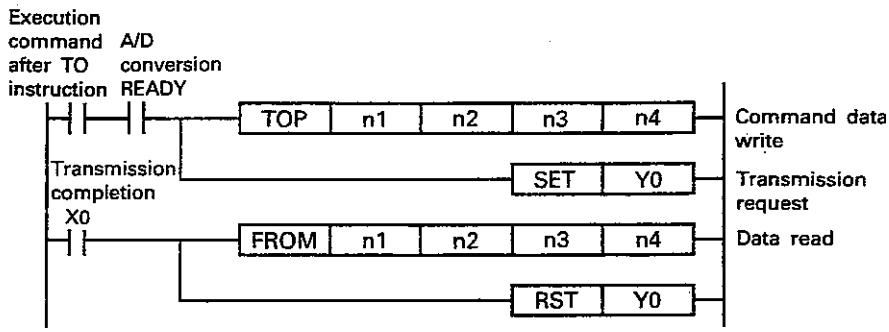
Command data and write data are set as follows.



5.6.2 Reading data from the A68ADC

The FROM instruction is used to read data, which was transmitted from the buffer memory of designated remote terminal module, from the remote terminal receive areas of the master module using the TO instruction in the sequence program.
Items of the buffer memory and procedures of reading from the A68ADC are described below.

(a) Digital output of each channel
(b) A/D conversion completion flag
(c) Write data error code



Command data write format (TO instruction)

n1	Head I/O number assigned to AJ71PT32-S3
n2	Head address of the remote terminal transmission areas of corresponding remote terminal number assigned by initial data.
n3	Head device number of data register which stores command data.
n4	Total number of words of command data

Command data is set as follows.

Head device designated by n3 → n3	1	Read command code: 1
n3+1	10	Read head address of A68ADC buffer memory: 10
n3+2	3	Number of read data words: 3

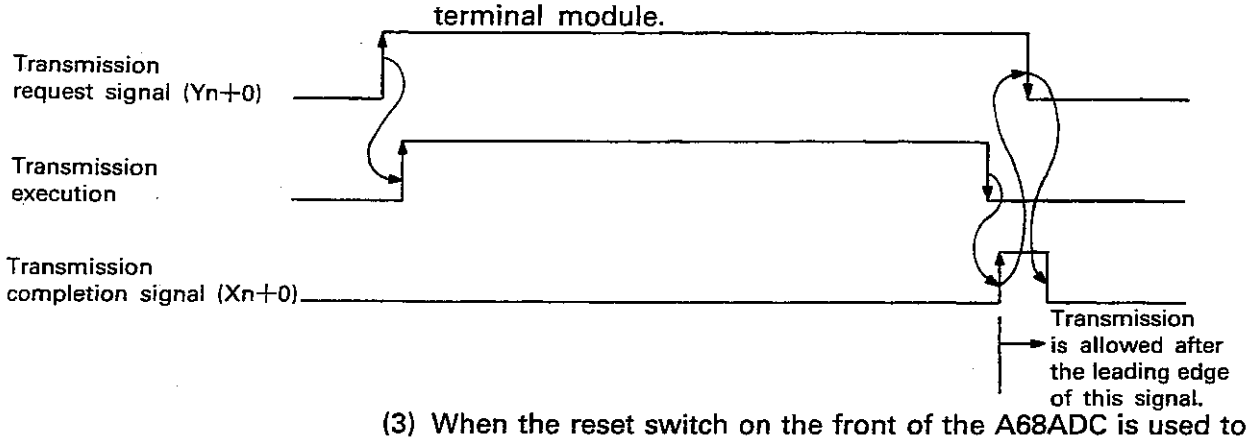
Data read format (FROM instruction)

n1	Head I/O number assigned to AJ71PT32-S3
n2	(Head+1) address of the remote terminal receive areas of corresponding remote terminal number assigned by initial data.
n3	Head device number of data register which stores receive data.
n4	Total number of words of read data

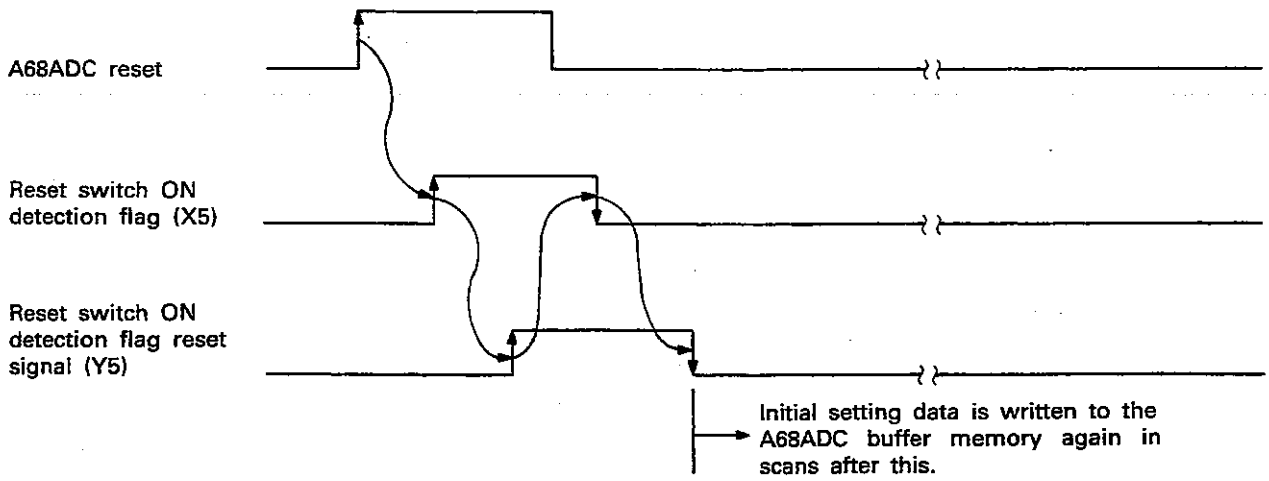
5.6.3 Cautions on programming

(1) For communication with the remote terminal modules linked to the AJ71PT32-S3, turn ON the AJ71PT32-S3 communication start signal $Y_{(n+28)}$ always before execution of each instruction. If the communication start signal has not turned ON, communication processings are not possible.

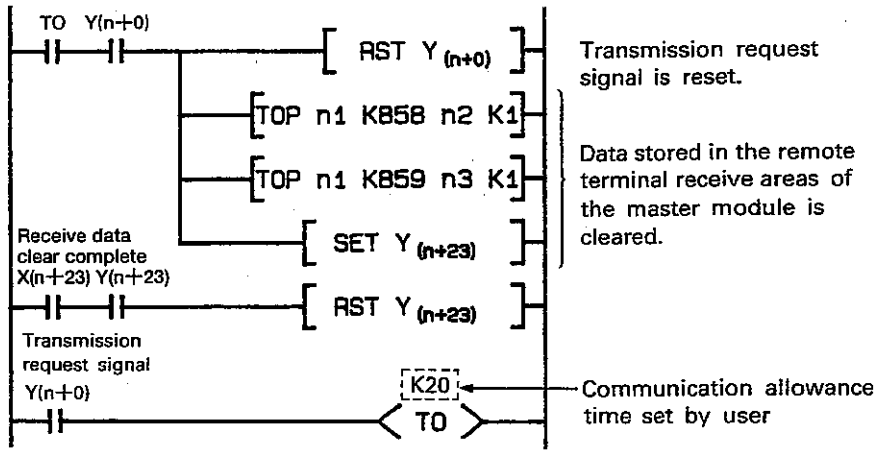
(2) Transmission to a remote terminal module cannot be performed if the transmission request signal previously assigned to the same module remains turned ON. Confirm that the previous transmission is completed with the transmission completion signal, and then, reset the transmission request signal before executing transmission to the same remote terminal module.



(3) When the reset switch on the front of the A68ADC is used to reset, the A68ADC returns to initial state. Processings are executed with defaults till new set data such as channel designation and averaging processing designation is written to the buffer memory.
The reset switch ON detection signal from the A68ADC should always be read from the batch refresh receive areas of the master module using the FROM instruction. Initial set data should be transmitted to the A68ADC when the detection signal has turned ON.



(4) If a communication completion response signal to the transmission executed to the A68ADC is not sent back, the CPU module is set in the state waiting for the communication completion signal infinitely unless the CPU module is reset. To prevent the infinite completion wait state, provide a monitoring timer to turn off the transmission request signal and to clear data stored in the remote terminal receive areas when the timer has timed out, as shown below.

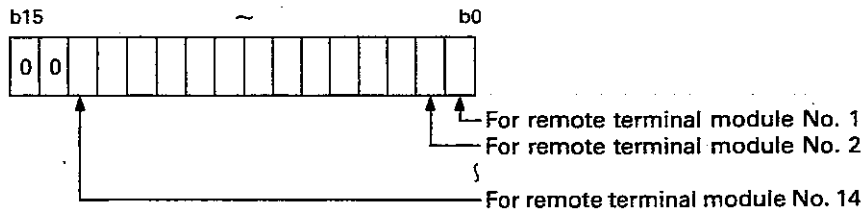


$X_{(n+28)}$, $Y_{(n+0)}$ and $Y_{(n+23)}$ are control I/O signals for the AJ71PT32-S3. See Section 5.3.2 for details.

Contents of n_1, n_2 and n_3 designated by each instruction are as described below.

n_1: Higher 2 digits of head I/O number assigned to AJ35PT32-S3
Example) "12_H" when assigned to X/Y120 to 13F.

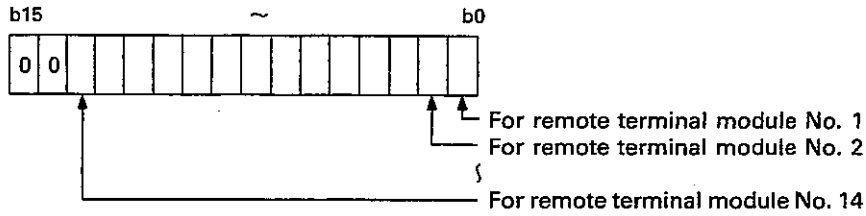
n_2: Receive buffer clear/no clear setting for each remote terminal number



0: No clear
1: Clear

Contents of setting are written to address 858 in the AJ71PT32-S3 buffer memory.

n3: Clear execution range setting for each remote terminal number

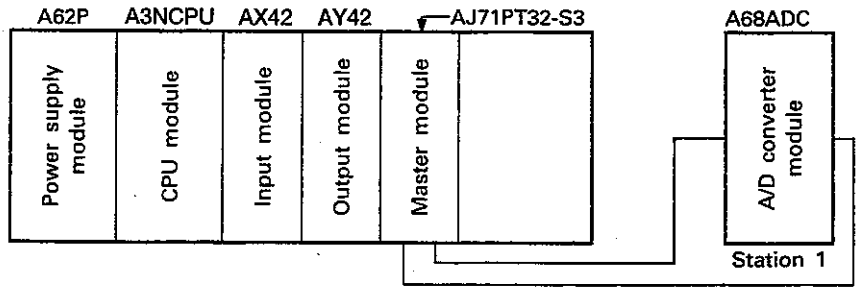


0: Only the remote terminal receive areas of the master module are cleared.
1: The remote terminal receive areas of the master module and the A68ADC receive buffer are cleared.

Contents of setting are written to address 859 in the AJ71PT32-S3 buffer memory.

5.6.4 Programming example

The following is a programming example when the digital output values of channels 1 and 2 of the A68ADC are always read in the system configuration shown below.
Channel 1 is set for averaging by time (500 ms) and channel 2 is set for averaging by count (100 times). Channels 3 to 8 are not set for A/D conversion.

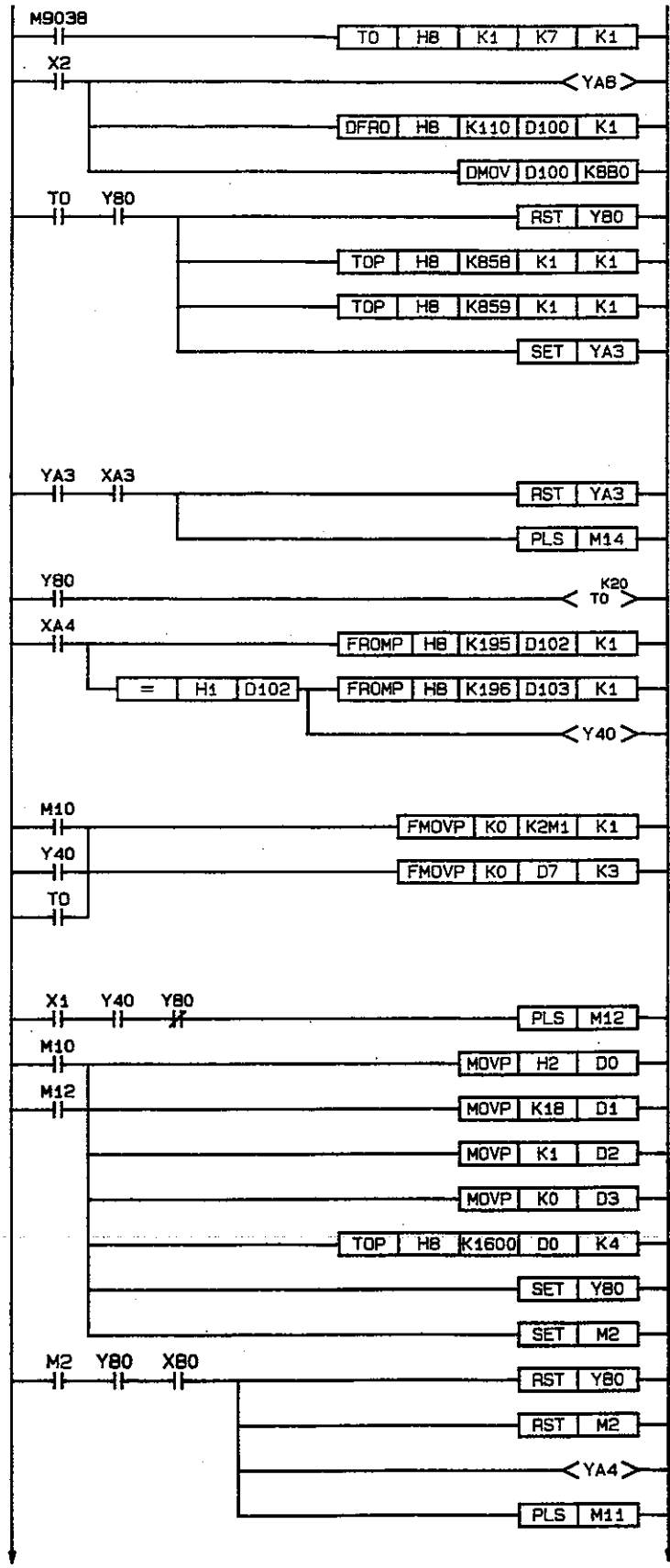


1) Contents of initial data ROM setting

Total of linked stations: 4
Number of remote terminals: 1
Remote terminal No. 1: Station 1
Protocol: MINI standard
FROM address: 0
TO address: 500

2) Programming

- When X2 (MINI-S3 link communication start instruction) of the input module has turned ON, the MINI-S3 link starts.
- A/D conversion starts when the MINI-S3 link communicating signal has turned ON. When X0 (read start instruction) of the input module has turned ON, digital outputs are stored in D8 and D9.
- When an error is detected during communication with a remote terminal module, Y40 of the output module is turned ON to stop all processings.
  When X1 (communication error detection flag reset instruction) is turned ON, the error code storage areas and flags are all cleared.
- When the A68ADC is reset with the reset switch, all processings are stopped. When X2 (reset switch ON detection flag reset instruction) is turned ON, all flags are cleared.



Retry count "7" is set at buffer memory address 1 of the master module.

When the MINI-S3 link communication start request (X2) has turned ON, the MINI-S3 link starts communication, and the A68ADC control input signals are always read to B0 to B1F.

The following processings are executed when the communication response monitoring timer has counted up.
(1) Y80 (transmission request signal to remote terminal module No. 1) is turned OFF.
(2) Clear of the remote terminal module No. 1 receive area of the master module is designated and the receive data clear request signal (YA3) is set.

M14 is turned ON by the receive data clear completion (XA3) and the receive data clear request (YA3) is reset.

Communication response monitoring time is set by user.

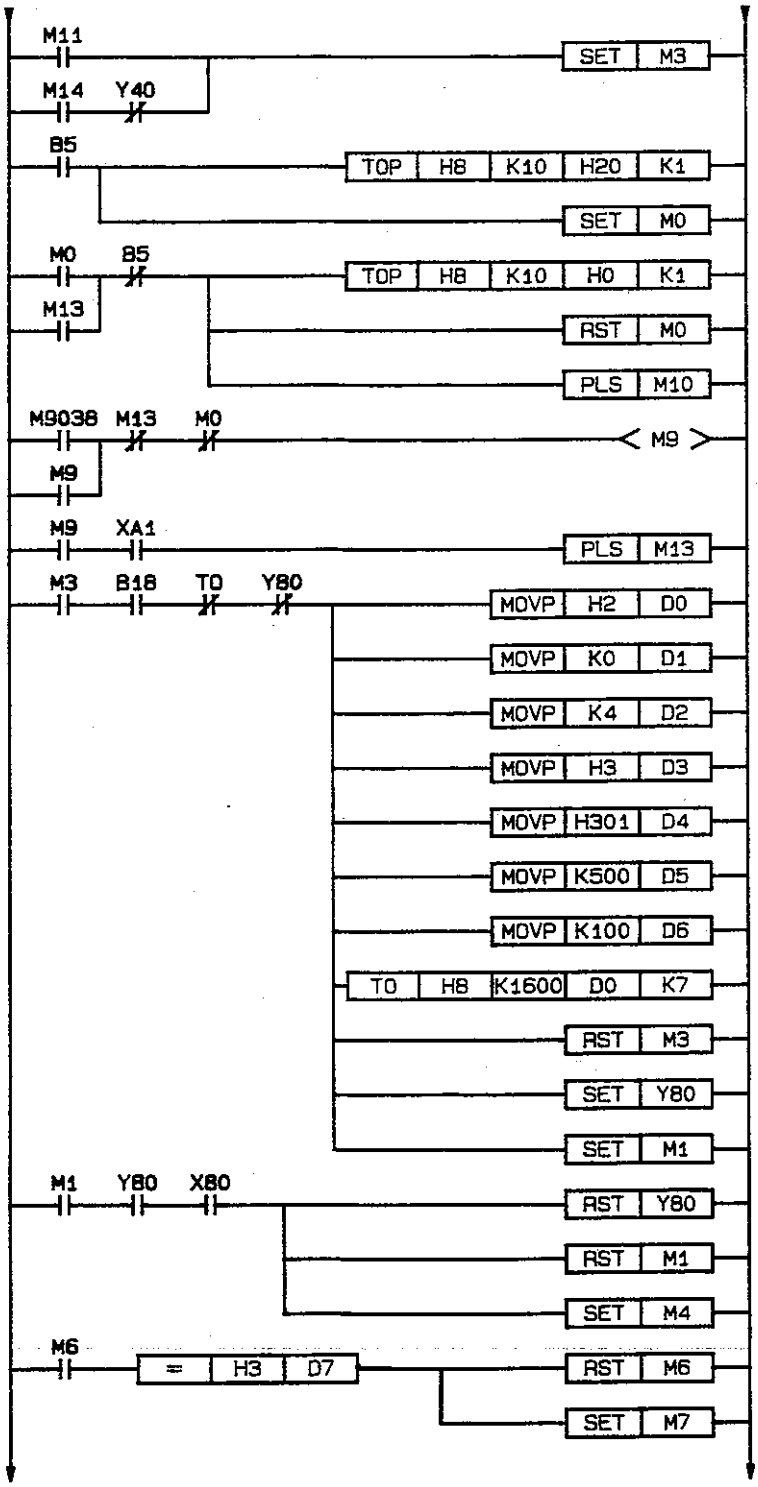
Error of remote terminal module No. 1 is indicated on external devices (Y40) and corresponding error code is read to D103.

Device clear is executed when any of the following conditions are established.
(1) The CPU is reset or the reset switch ON detection flag of the A68ADC is reset.
(2) Communication error occurs.
(3) Communication response monitoring timer counts up.

Communication error reset command

Data D0 to D3 are written to the remote terminal No. 1 transmission areas of the master module and the transmission request signal (Y80) is set.
D0: Write command code
D1: A68ADC buffer memory address
D2: Number of write data words
D3: Write data

The following processings are executed when transmission to remote terminal No. 1 is completed.
(1) Transmission request signal is reset.
(2) Remote terminal error detection is reset.
(3) M11 is turned ON when communication error reset is completed.



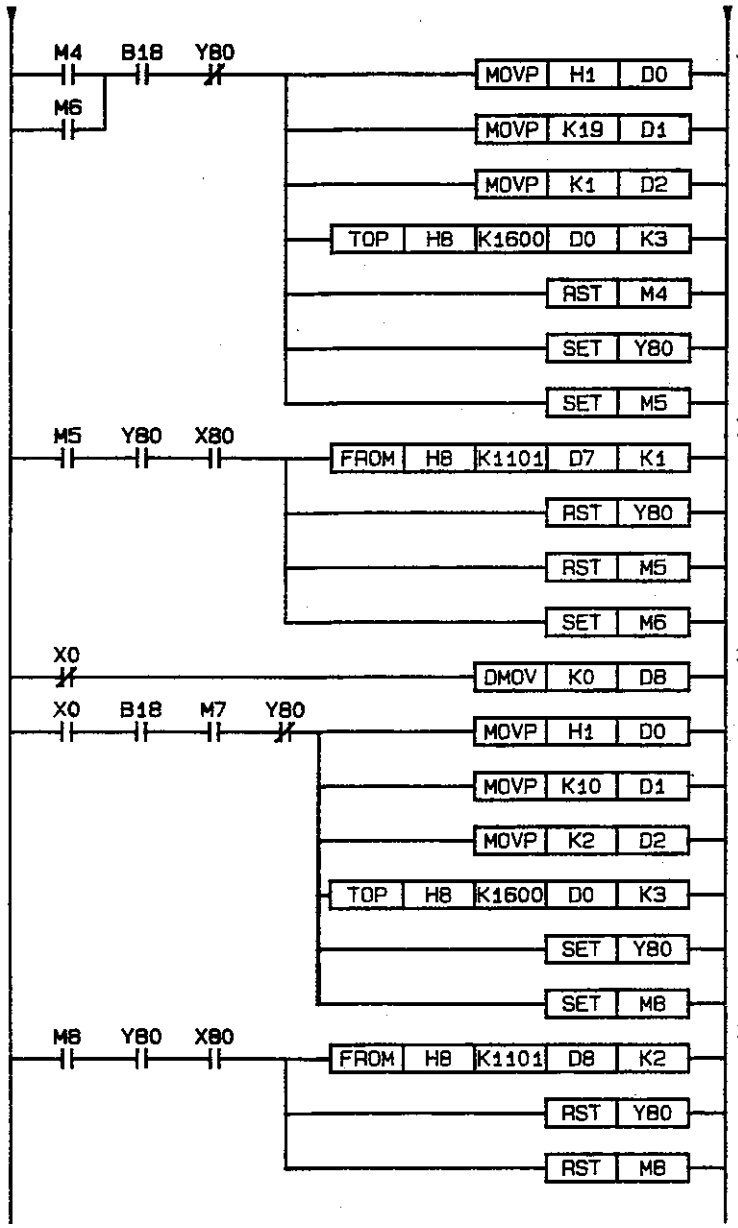
The A68ADC initial setting command (M3) is set when communication error reset is completed or receive data clear is completed.

(1) The reset switch ON detection flag set by hardware reset of the A68ADC is reset.
(2) M10 is turned ON when the above processing is completed or the CPU is reset.

Data D0 to D6 are written to the remote terminal No. 1 transmission areas of the master module and the transmission request signal (Y80) is set.
D0: Write command code
D1: A68ADC buffer memory head address
D2: Number of write data words
D3: Channel designation CH1/CH2
D4: Averaging processing designation
D5: CH1=500 ms } Averaging processing
D6: CH2=100 counts }

The following processings are executed when transmission of data set with M1 is completed.
(1) The transmission request signal for remote terminal No. 1 (Y80) is reset.
(2) A/D conversion completion flag read command (M4) is set.

When A/D conversion is completed (3H) on both CH1 and CH2, A/D conversion completion flag read is stopped and digital output read command (M7) is set.



Data D0 to D2 are written to the remote terminal No. 1 transmission areas of the master module and the transmission request signal (Y80) is set.
D0: Read command code
D1: A68ADC buffer memory address
D2: Number of read data words

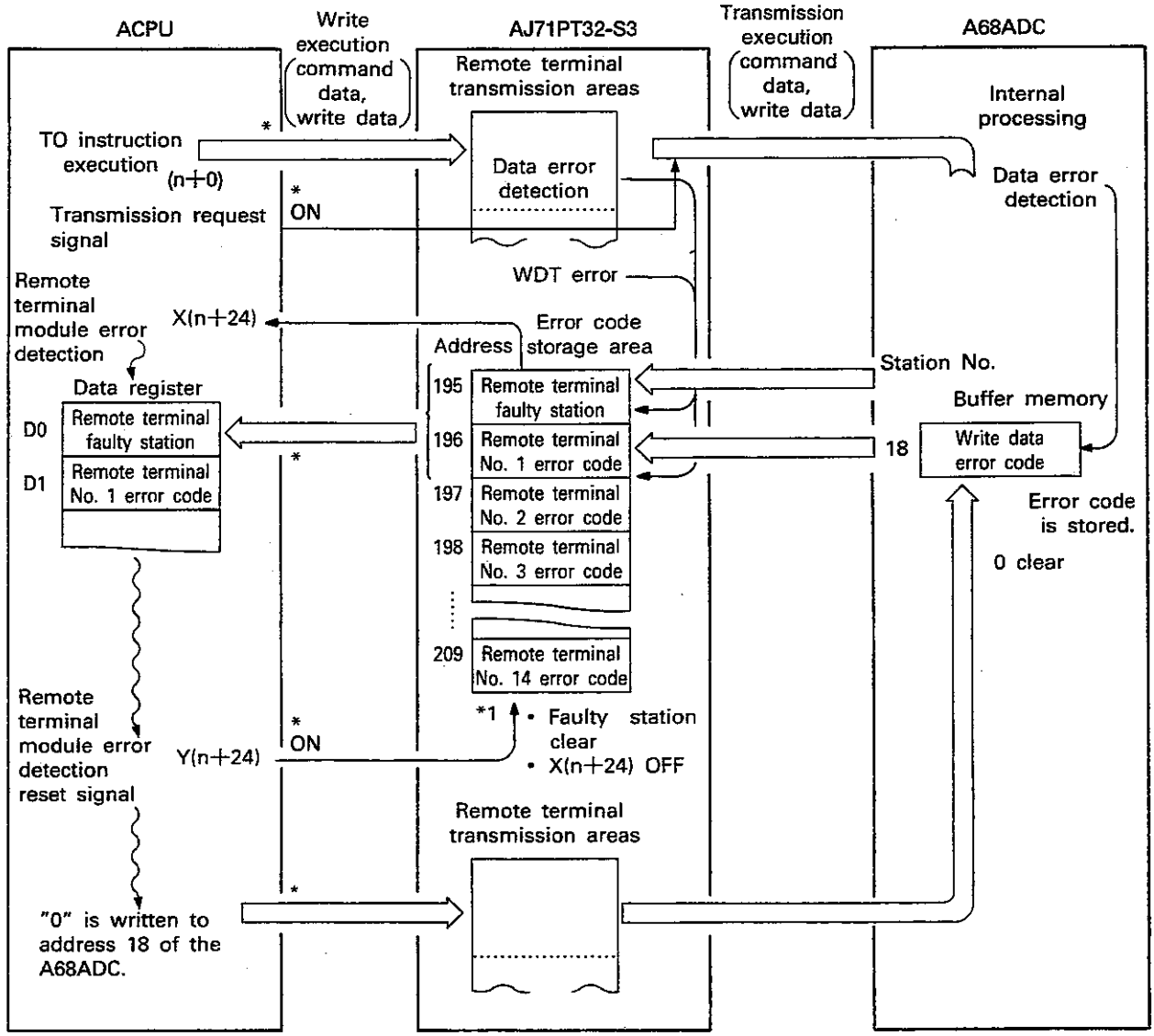
The following processing is executed when transmission to the A68ADC is completed.
(1) Data is read to D7 from the remote terminal No. 1 receive areas of the master module.

Digital output values of CH1 and CH2 are read to D8 and D9 by turning ON the digital output value read command (X0).
Data D0 to D2 are written to the remote terminal No. 1 transmission areas of the master module and the transmission request signal (Y80) is set.
D0: Read command code
D1: A68ADC buffer memory head address
D2: Number of read data words

Digital output values are read to D8 and D9 from the remote terminal No. 1 transmission areas of the master module by turning ON the transmission completion signal (X80).

5.7 Error Detection

The diagram below shows the detecting procedure when errors have occurred when the ACPU, A68ADC and AJ71PT32-S3 are used together.



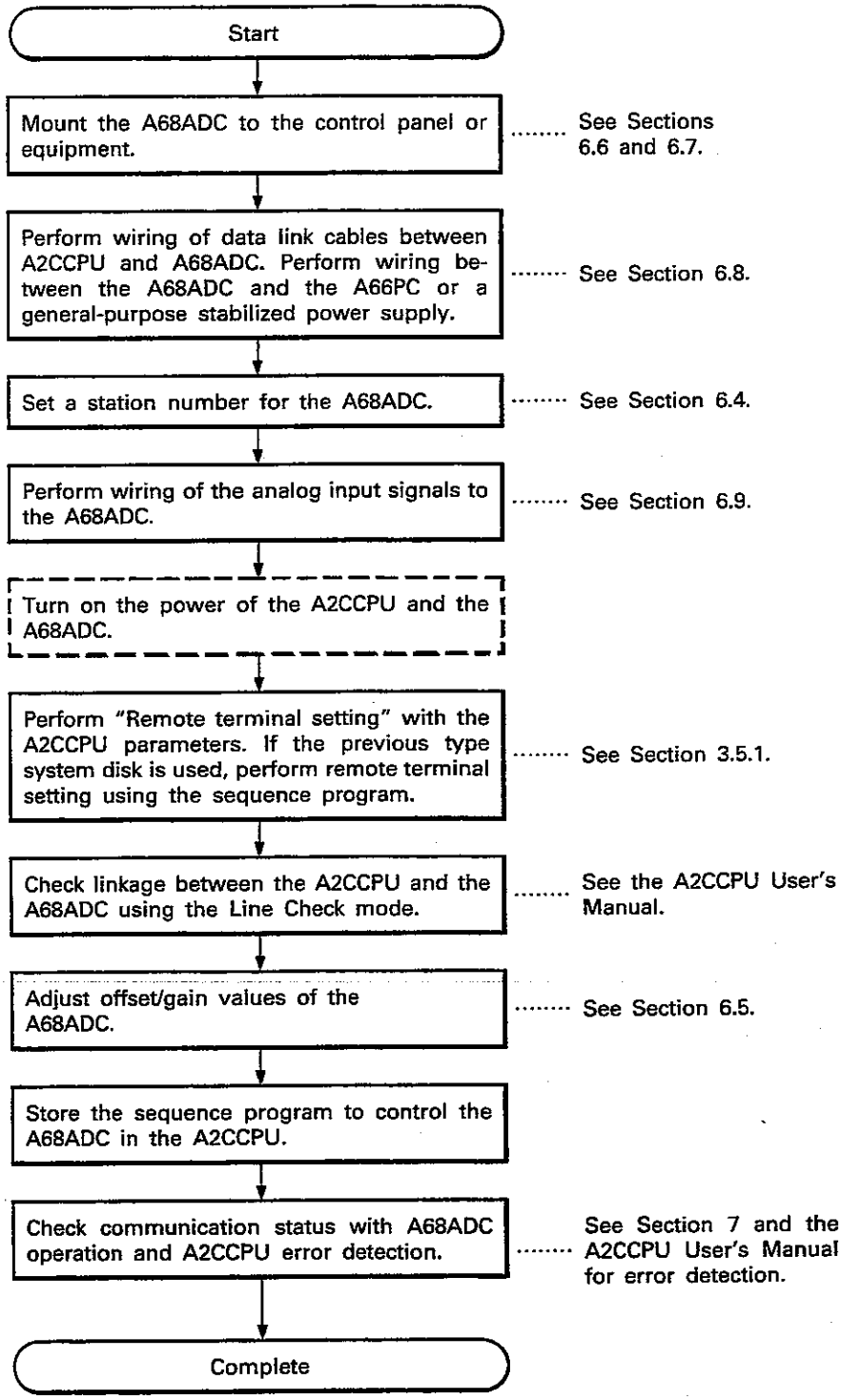
Processings marked * by an asterisk are executed by the sequence program.

6. INSTALLATION AND PRE-OPERATION SETTING PROCEDURES

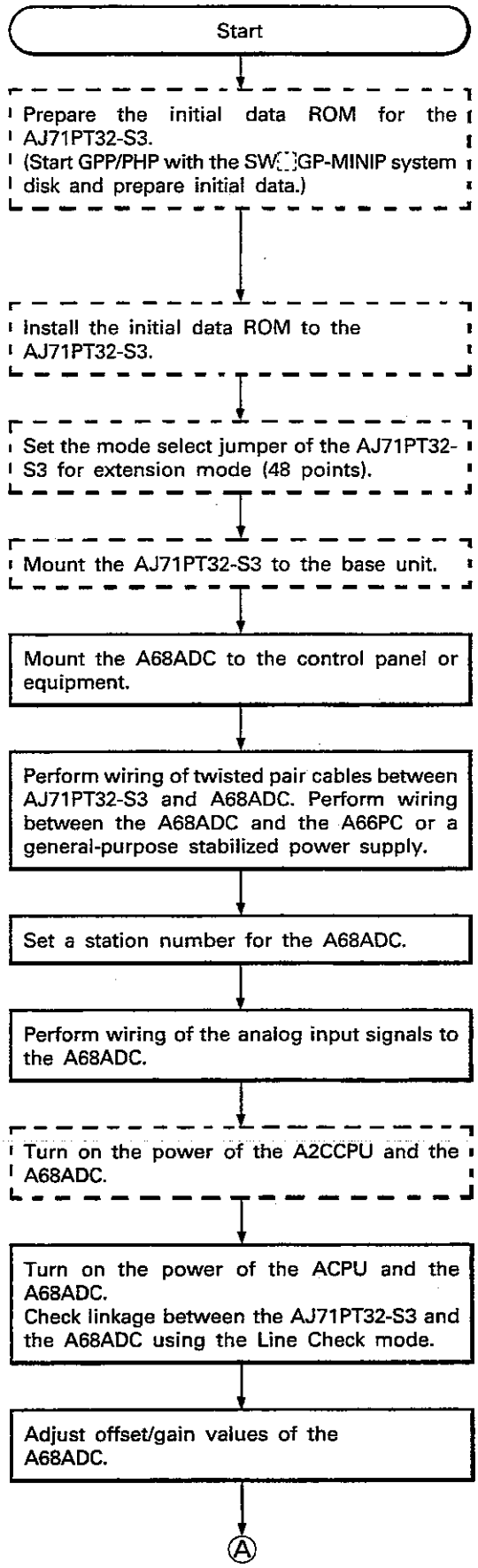
6.1 Pre-operation Setting Procedures

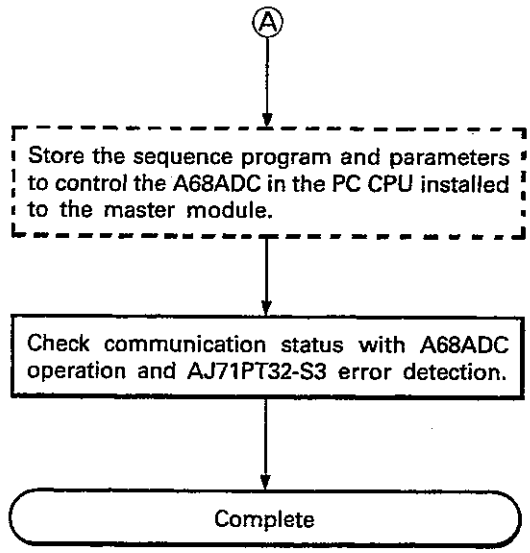
This section gives setting procedures required before starting operation of the A68ADC when used with the A2CCPU and with the AJ71PT32-S3.

(1) When the A2CCPU is used:



(2) When the AJ71PT32-S3 is used:





See Sections 4.5.2 and 4.6 when the AnACPU is used.
See Section 5.6 when a CPU of other than the AnA type is used.

See the AJ71PT32-S3 MELSECNET/MINI-S3 Master Module User's Manual for error detection.

6.2 Handling Instructions

(1) Protect the A68ADC and its terminal block from impact.

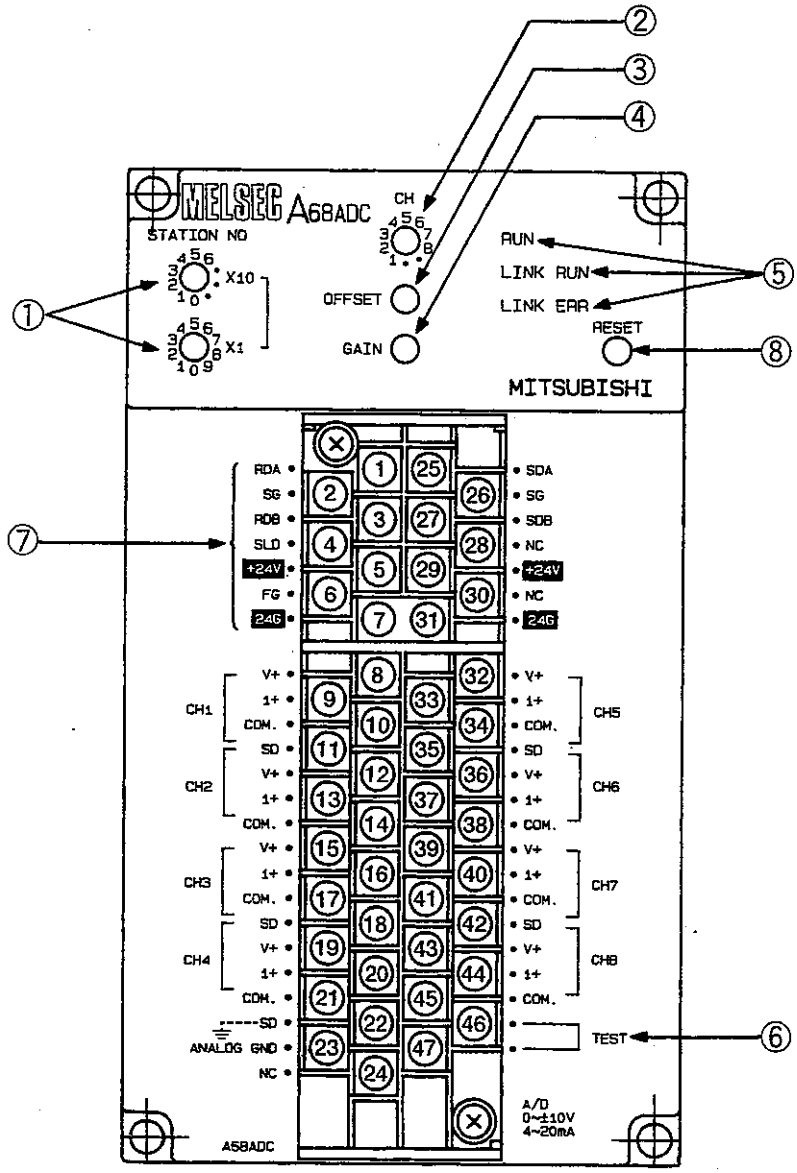
(2) Do not touch or remove the printed circuit board from the case.

(3) When wiring, ensure that no wire offcuts enter the module and remove any that do enter.

(4) Tighten terminal screws as specified below.

Screw	Tightening Torque Range N·cm
I/O terminal block terminal screw (M3.5 screw)	59 to 88
I/O terminal block mounting screw (M4 screw)	78 to 118

6.3 Part Identification



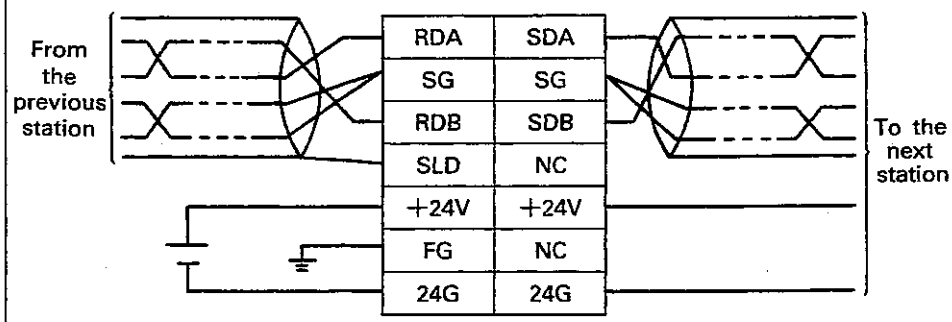
<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>Station number setting switches</td><td>①×10
①×1
Used to set the station number of the A68ADC in a range from 1 to (64 − occupied stations + 1).
See Section 6.4.</td></tr>
<tr><td>2</td><td>Channel select switch</td><td>Used to select the channel for offset/gain adjustment.
(Positions 0 and 9 select no processing.)</td></tr>
<tr><td>3</td><td>OFFSET switch</td><td>By turning this ON in the TEST mode (short the TEST mode terminals), the analog input value at that time is stored as the offset value in the A68ADC.</td></tr>
<tr><td>4</td><td>GAIN switch</td><td>By turning this ON in the TEST mode (short the TEST mode terminals), the analog input value at that time is stored as the gain value in the A68ADC.</td></tr>
<tr><td>5</td><td>Operation state indicator LEDs</td><td>
<table>
<tr><td rowspan="2">RUN LED</td><td>Normal mode</td><td>On: Normally running
Flicker: Write data error
Off: 24 VDC is off or WDT error.</td></tr>
<tr><td>Test mode</td><td>On: OFFSET or GAIN switch is ON.
Off: OFFSET or GAIN switch is OFF.</td></tr>
<tr><td>LINK RUN LED</td><td>On:
Off:</td><td>Normal communication
Receive data error</td></tr>
<tr><td>LINK ERR LED</td><td>On:
Off:</td><td>Receive data error
Normal communication</td></tr>
</table>
</td></tr>
<tr><td>6</td><td>Test mode terminals</td><td>Shorted when setting offset/gain.</td></tr>
<tr><td>7</td><td>Terminal block for twisted pair cables and power supply cables</td><td> 
</td></tr>
<tr><td>8</td><td>Reset switch</td><td>Hardware reset
Used to initialize buffer memory and operation processing of the A68ADC.
By turning this ON, the control input signal X5 of the A68ADC turns ON.
(Device number of control I/O signals depends on station setting.)</td></tr>
</table>

Table 6.1 Names and Description of Parts

6.4 Station Setting

By setting the station number of the A68ADC, addresses of the batch refresh communication areas where control I/O signal information is stored and the range of use of the remote terminal communication data areas where command data and read/write data are stored are designated. Perform station setting considering the following.

POINT

Do not change station setting during communication in the MINI-S3 link. If changed, output or input error may occur.

(1) The range of station setting is 1 to (64—[number of occupied points of this module]+1).

(2) The range of communication with remote I/O modules and remote terminal modules is determined by the total number of remote stations (initial data ROM).
For example, when the total number of remote stations is 10, communication is executed with the remote I/O modules and remote terminal modules of which station numbers are between 1 and 10.

(3) Station numbers can be set without regard to the order of connection of modules.
For example, station setting shown in Fig. 6.1 is allowed.

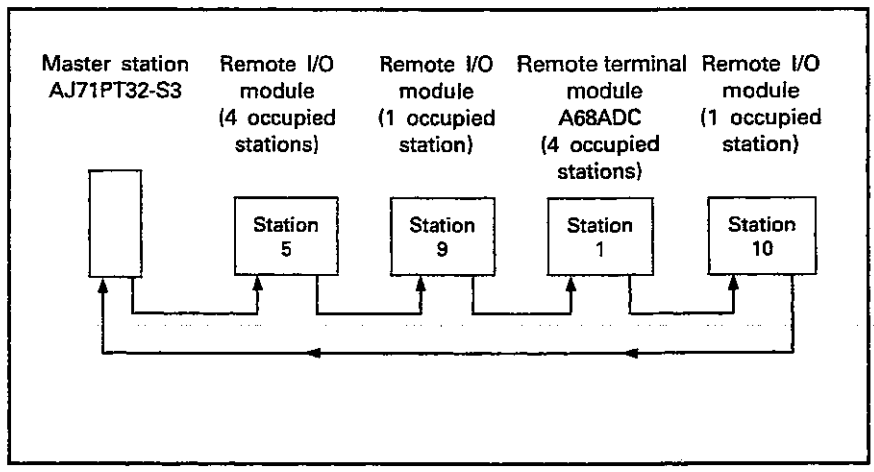


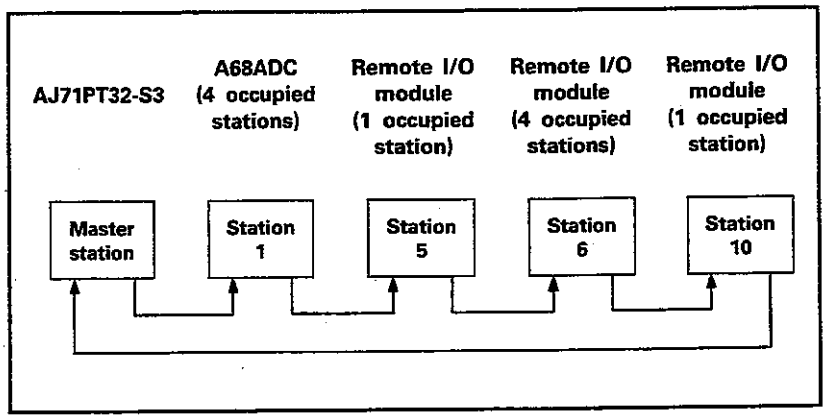
Fig. 6.1 Remote Module Station Setting

(4) Set station numbers not to leave unused stations (station numbers which correspond to no remote terminal module or remote I/O module).
f there is an unused station within the total number of remote stations (set with the initial data ROM), such station is detected as a communication error station.

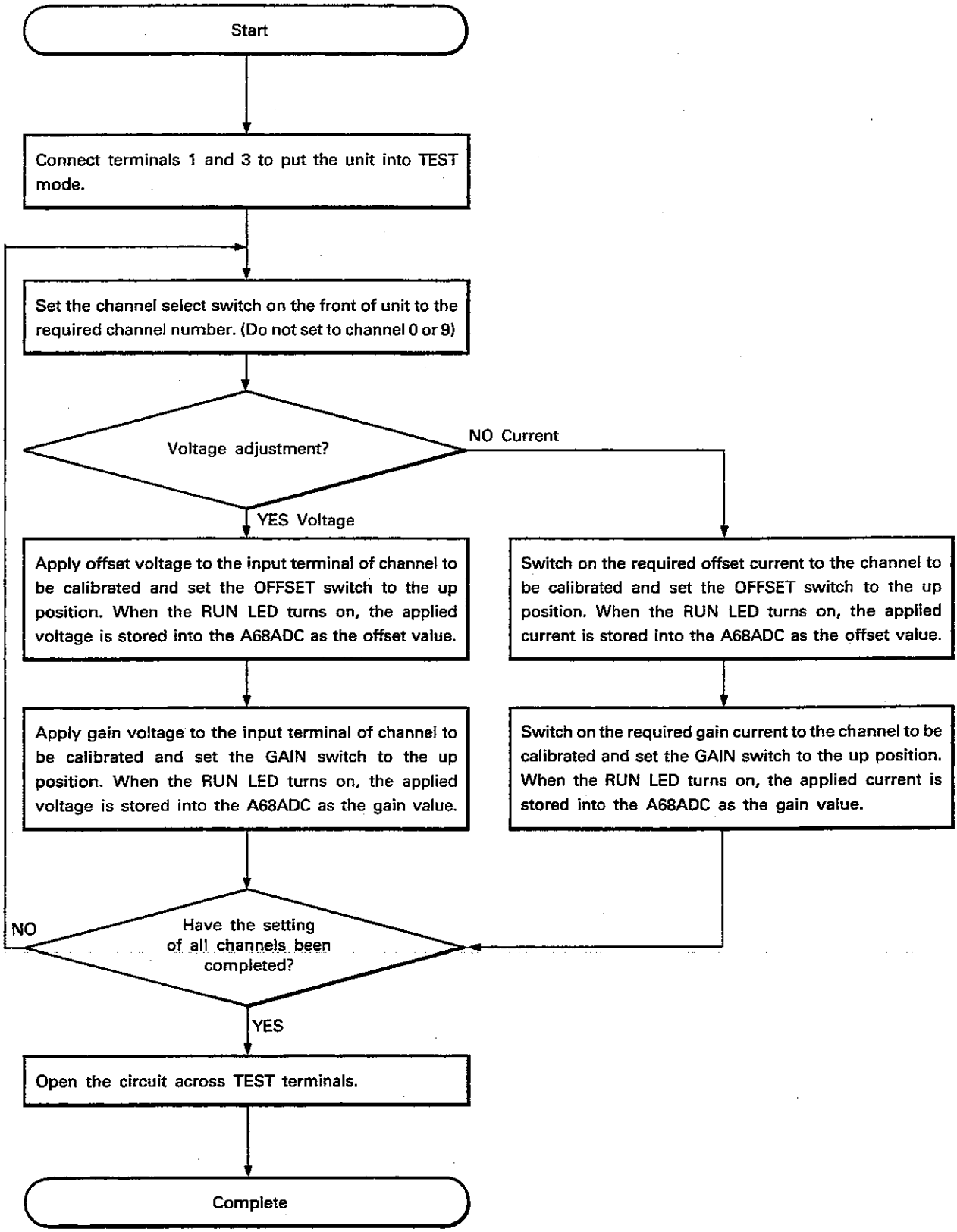
POINT

(1) Do not set any two or more stations for one same station number in the same loop. If two or more stations are set for the same station number, such stations may not operate normally. Make sure that there are no stations assigned with the same station number.

(2) If remote terminal or I/O modules which have two or more occupied stations are used, set station numbers skipping the numbers used for occupied stations. For example, if the A68ADC which has four occupied stations is set for station 1, shown below, do not set other remote I/O modules for stations 2, 3 and 4.



6.5 Offset/gain Setting



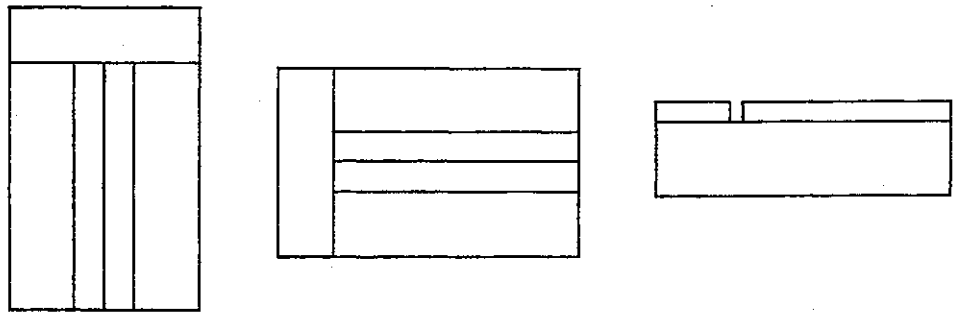
POINT

(1) Set the offset and gain values under the condition of actual use.
(2) The offset value and gain value are stored in the A68ADC and are not erased if the power is turned off.
(3) Perform the offset/gain setting with the CPU in stop mode. When the unit is set to test mode, A/D conversion is stopped on all channels. Therefore, use the A/D conversion ready signal as an interlock.
(4) Perform the offset/gain setting within the range −10 to 0 to +10 VDC or −20 to 0 to +20 mADC. If set outside this range, the maximum resolution and overall accuracy may not be within the ranges specified.
(5) If grounding at the point marked with *5 described in Section 6.9.2 (no ground → ground, or ground → removal), perform offset/gain setting again from the first step.

6.6 Mounting Directions

(1) The A68ADC can be mounted in any direction (Front side must not face downward.)

(2) Examples



Upright Horizontal Front side up

6.7 Mounting to the DIN Rail

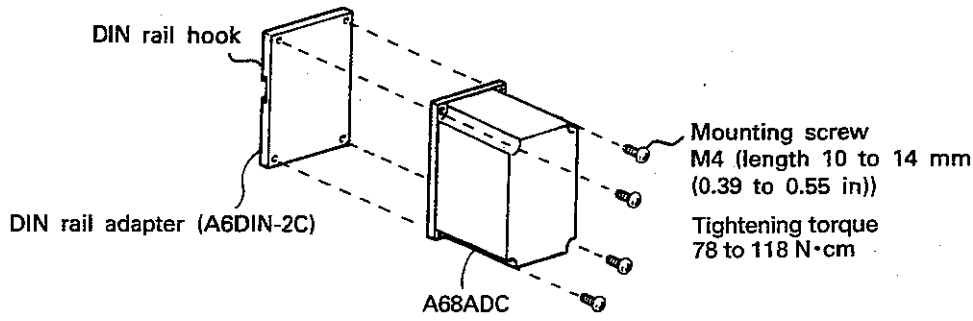
6.7.1 Fixing a DIN rail adapter to a module

(1) Specifications
Table shows specifications of the DIN rail adapters.

Item \ Type	A6DIN2C
Applicable module	A68ADC, special function module for others and A2C CPU
External dimensions mm (in)	106 (2.68) × 174 (6.85)
Weight kg	0.06

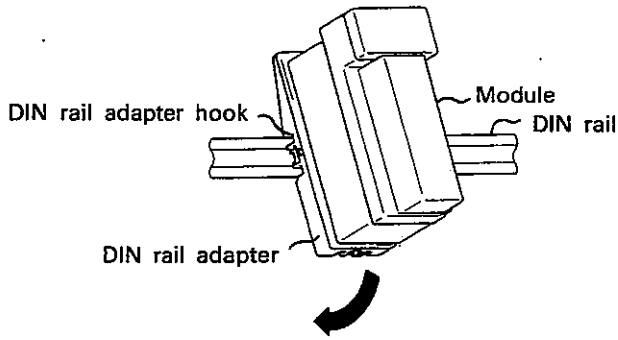
(2) Handling instructions
- Do not drop or give hard shocks to the DIN rail adapter since it is made of plastic.
- Use M4 screws of 10 mm (0.39 in) to 14 mm (0.55 in) long to fix a DIN rail adapter to a module. Torque range should be 78 to 118 N·cm.

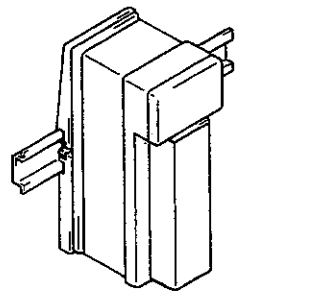
6.7.2 Fixing a DIN rail adapter to a module



6.7.3 Mounting to the DIN rail

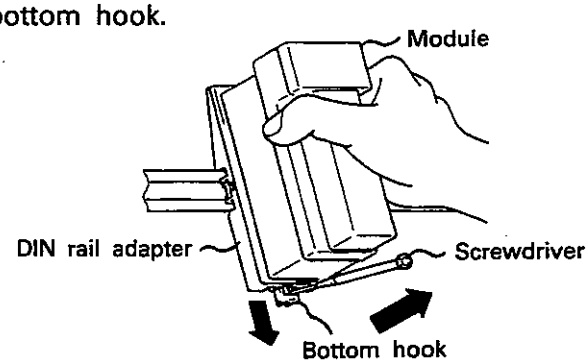
(1) Mounting procedure
After fixing the DIN rail adapter to the module, mount the module to the DIN rail as follows.
a) Engage the hook of the adapter with the rail from above the rail.
b) Push the module onto the rail and fix it in position.




A module mounted to DIN rail

c) When two adapters with module are mounted to the rail side by side without leaving a clearance between them, a 4 mm clearance is allowed between the modules.

(2) Removing procedure
Remove the module from the DIN rail as follows.
a) Pull down the bottom hook of the adapter using a screwdriver.
b) Pull the module away from the rail while pulling down the bottom hook.



Pull to remove.

6.8 Wiring of Data Link Cables

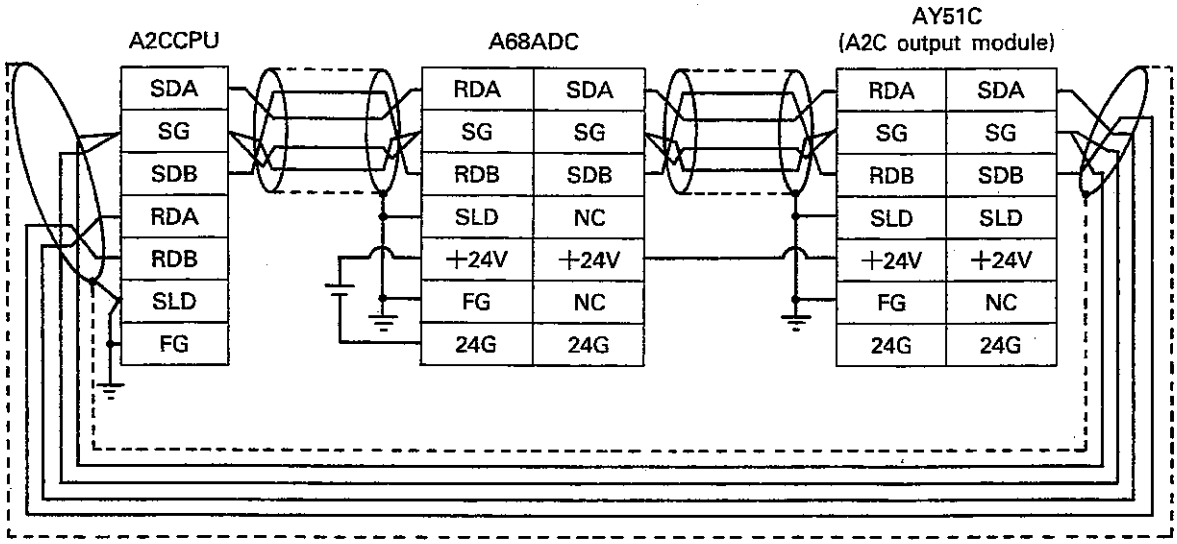
6.8.1 Handling instructions for twisted pair cables

Handle cables with special care.

(1) Do not compress the cable with rigid and sharp-edged material.
(2) Do not twist the cable extremely.
(3) Do not tense strong the cable.
(4) Do not step on the cable.
(5) Do not put things on the cable.
(6) Do not damage the insulation of the cable.

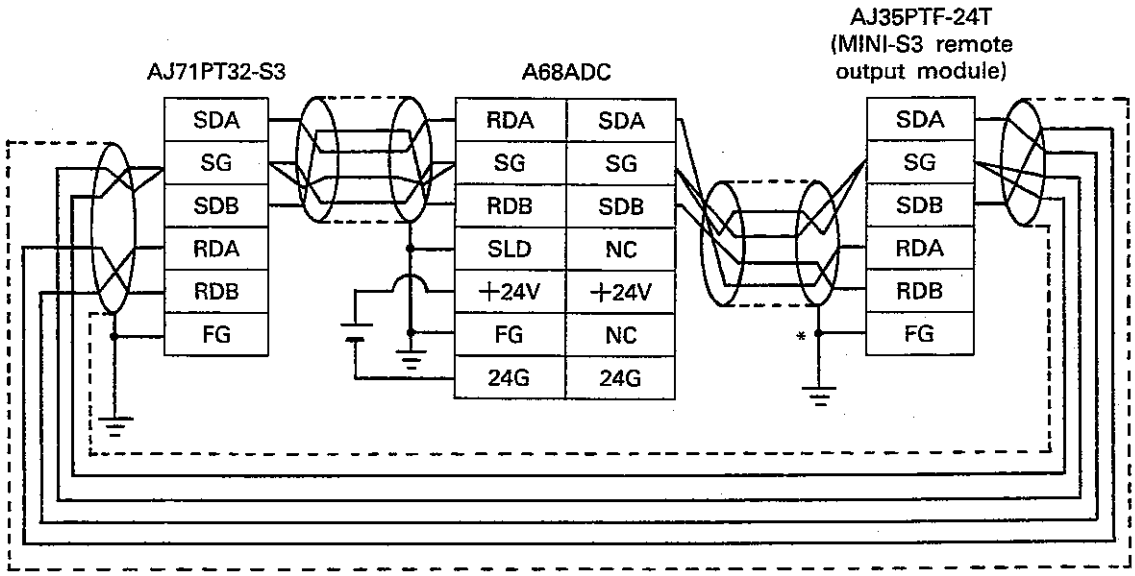
6.8.2 Connection of twisted pair cables

(1) Connecting the A2CCPU and the A68ADC



* Ground the shields at one point.

(2) Connecting the AJ71PT32-S3 and the A68ADC



* Ground the shields at one point.

The twisted pair shield cable terminal block uses the terminal screws shown below. Use appropriate solderless terminals.

Module Type	Terminal Screw	Tightening Torque Range N·cm
A2CCPU A68ADC A2C I/O module	M3.5	59 to 88
MELSECNET/MINI-S3 remote I/O module (batch refresh type)	M4	98 to 137

POINT

Twisted pair cables must be connected so that they may not be influenced by noise or serge induction.

(1) Do not lay the cables close to nor bind them together with main circuit wires, high-tension wires or load carrying wires. (allow 100 mm or more clearance)

(2) When connecting to the remote module terminal block, allow maximum clearance between twisted pair cables and module power supply lines and I/O signal wires.

(3) Do not use a part of twisted pair cables (such as one pair among 3 pairs) for power supply.

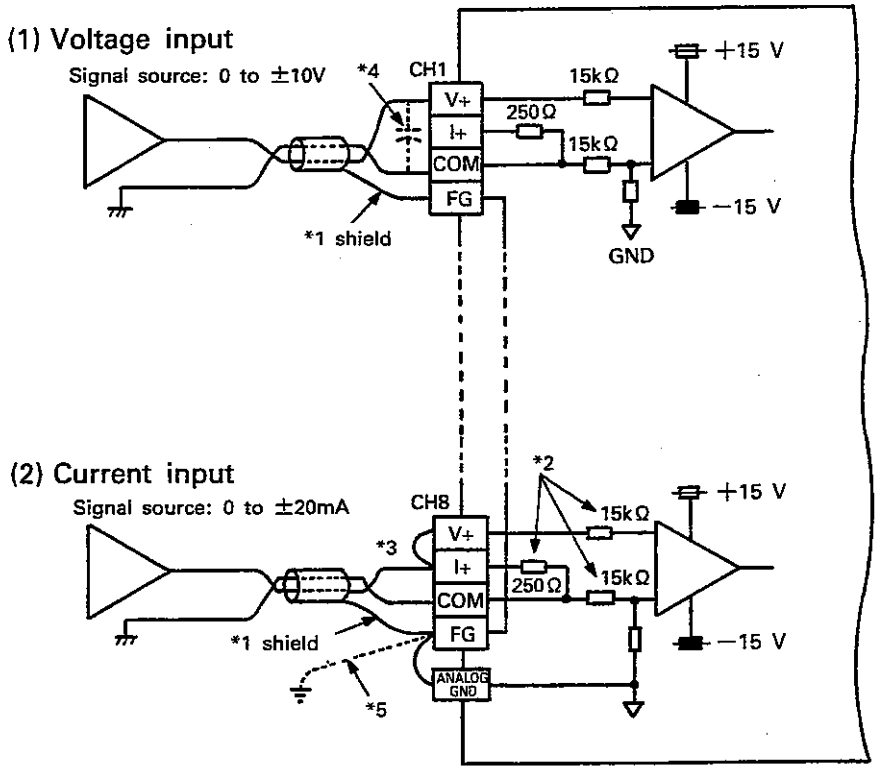
6.9 Wiring of Analog Input Signal Cables

6.9.1 Wiring instructions

Protect external wiring against noise with the following precautions:

(1) Separate AC and DC wiring.
(2) Separate main circuit and/or high voltage wiring from control and signal wiring.
(3) Where applicable, ground the shielding of all wires to a common ground point.

6.9.2 Module connection example



*1: For the cable, use a two-core twisted shielded wire.
*2: Indicates the input resistance of the A68ADC.
*3: For current input, be sure to connect the terminals (V+) and (I+).
*4: **If noise or ripple is generated at the external wiring, connect a capacitor of approximately 0.1 to 0.47 μF (25V or more voltage resistance parts) between terminals V and COM.**
*5: If there is excessive noise, ground the module.
If any change has been made in grounding method (ground/no ground) after offset/gain setting, perform the setting again.

7. TROUBLESHOOTING

7.1 List of Error Codes

If an error has occurred when data is written to the A68ADC (the RUN LED flickers), any of the error codes mentioned in the list below is stored in buffer memory at address 18.
When the A2CCPU is used, the same error code is stored also in special registers D9180 to D9193. When the AJ71PT32-S3 is used, the same error code is stored also in buffer memory at addresses 196 to 209.

Error Code	Cause	Corrective Action
100 (64H)	(Read error) • Designated head address is out of buffer memory. • Designated range of read words includes addresses out of buffer memory.	Correct data which designates range out of buffer memory.
101 (65H)	(write error) • Designated head address is out of buffer memory. • Designated range of write words includes addresses out of buffer memory. • Write was attempted to read-only areas.	• Correct data which designates range out of buffer memory. • Correct data which designates range read-only areas.
102 (66H)	Command code other than read (1) or write (2) is received.	Probably due to noise interference. Implement noise countermeasures.
103 (67H)	Data was received immediately after read command (1).	
104 (68H)	Read and write word length is set at "0".	
105 (69H)	The number of words set by write command data differs from that of received data.	
1 ⬚ 0 to 4	Averaging time is set out of 20 to 10000 msec range. • ⬚ indicates the channel in which the error occurred. • Numbers 0 to 4 do not have meaning, but indicate an averaging time error.	Correct averaging time setting in 20 to 10000 msec range.
1 ⬚ 5 to 9	Averaging count is set out of 1 to 4000 counts. • ⬚ indicates the channel in which the error occurred. • Numbers 5 to 9 do not have meaning, but indicate an averaging count error.	Correct averaging count setting in 1 to 4000 counts range.

Table 7.1 List of Error Codes (Errors Detected by the A68ADC)

(a) If two or more errors occur continuously, the error code for the first error is stored, and following error codes are not stored.

(b) Error code reset is done by writing "0" to address 18 of buffer memory. (Figures other than 0 are ignored.)

When the AJ71PT32-S3 is used, error codes for the errors occur during communication with remote terminal modules are stored in buffer memory at addresses 196 to 209 in addition to the error codes for errors detected by the A68ADC (Table 7.1).

Error Code	Error Name	Cause	Corrective Action
1	Set data error	Data written to the remote terminal transmission areas includes errors.	Correct the data.
6	WDT error	Remote terminal module malfunction.	• Reset faulty remote terminal module. • Turn OFF and then ON the power. • If the above procedures do not recover the system, the system hardware is faulty. Please consult Mitsubishi representative.
8	Transmission area setting error	Remote terminal transmission area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.
9	Communication error	Communication between the master module and remote terminal modules is faulty.	Noise or remote terminal module failure.
11 (B_H)			
10 (A_H)	Receive area setting error	Remote terminal receive area set range is smaller than the number of words used by remote terminal modules.	Correct initial setting data so that the set range is larger than the number of words used by remote terminal modules.

Table 7.2 List of Error Codes (Errors Detected by the AJ71PT32-S3)

7.2 When the RUN LED Flickers or Turned OFF

(1) When flickers:

Check Point	Corrective Action
Data which disables write or read is written to the A64DAVC/DAIC.	Refer to the List of Error Codes (Section 7.1) for the cause, and correct the sequence program.

(2) When turned OFF:

Check Point	Corrective Action
24 VDC power supply is turned on.	Make sure the power supply.
24 VDC power supply voltage is within the set range.	Adjust the voltage within 15.6 to 31.2 V range.
If the MINI-S3 link is connected, the MINI-S3 link communication start signal $Y_{(n+28)}$ is turned ON.	Add a loop to turn ON the MINI-S3 link communication start signal $Y_{(n+28)}$ to the sequence program.
If the MINI-S3 link is connected, error code "6" may be stored in the master module buffer memory at address 196 to 209.	Reset the PLC CPU, and start them in the same manner. If error code "6" is again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
If the MINI-S3 link is connected, error codes "9" and "10" may be stored in the master module buffer memory at address 196 to 209.	Reset the PLC CPU, and start them in the same manner. If error codes "9" and "10" are again stored, the system hardware may be faulty. Please consult Mitsubishi representative.
Data link cables are normal.	Check the cables referring to Section 6.8.
The TEST terminals are open.	After offset/gain setting, open the TEST terminals.

7.3 When the LINK RUN LED Turned OFF or the LINK ERR. LED Turned ON

Check Point	Corrective Action
The RUN LED is flickering.	Follow Section 7.2 (1).
The RUN LED turned OFF.	Follow Section 7.2 (2).

7.4 When Read of Digital Output Values is Impossible

Check Point		Corrective Action
The RUN LED is flickering or turned OFF.		Follow Section 7.2.
The ERROR LED of the CPU module is flickering or turned ON.		Refer to the User's Manual for respective CPU module for error content.
The RUN LED of the CPU module is flickering or turned OFF.		Refer to the User's Manual for respective CPU module for error content.
When A2CCPU is used:	The RD/SD LED of the CPU module is flickering. (normal)	Refer to the A2CCPU User's Manual for error content.
When AJ71PT32-S3 is used:	The MINI-S3 link communication start signal $Y_{(n+28)}$ is turned ON.	Set the sequence program to turn ON the MINI-S3 link communication start signal.
	The RUN LED of the master module is turned OFF.	Refer to the AJ71PT32-S3 User's Manual for error content.
	The RD/SD LED of the master module is flickering. (normal)	Refer to the AJ71PT32-S3 User's Manual for error content.
Analog input signal lines are broken or disconnected.		Locate trouble by checking the signal lines visually and for continuity.
Remove the wires for the A68ADC analog input, apply the test voltage to the terminal of the main unit and set the digital output value.		• If the digital output value at the A68ADC unit is normal, the external wiring is being affected by electrical noise. Check the wiring and installation. • Lift up the A68ADC from the frame and remove the installation wiring. (Use DIN rail mounting.)

APPENDICES

Appendix 1 I/O signal when combining Version B of A68ADC and Version B of A2CCPU.

(1) Communication error detection flag (Xn+4), communication error reset signal (Yn+4).

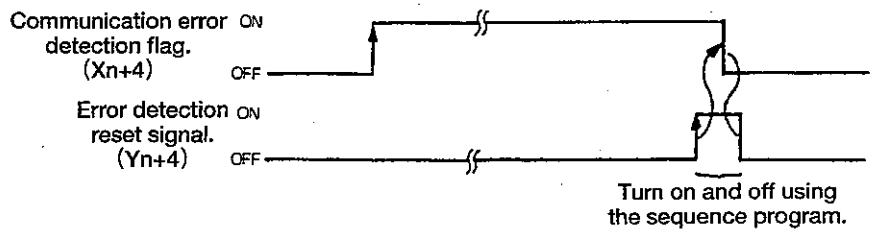
Reads from A2CCPU to A68ADC and if there is reading of command data that the reading cannot execute, it is set to on (latch).

(A68ADC RUN LED flashing)

Xn+4 is set to on and the error code (refer to Section 7.1, Table 7.1) is stored in the error code storage area (A2CCPU special register D9180 to D9193) for the corresponding remote terminal number.

After the communication error reset signal (Yn+4) is set to on by the sequence program, A68ADC is reset by the writing of "0" in address 18 of the A68ADC and the RUN LED comes on.

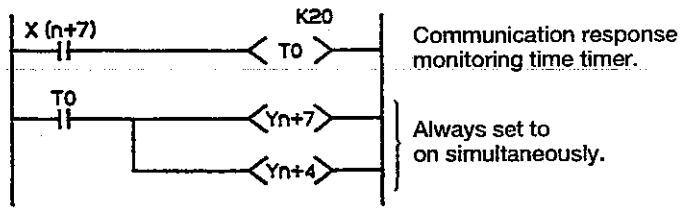
When the communication error reset signal (Yn+4) is set to on, the error code in the error code storage area (D9180 to D9193) and the corresponding FROM/TO instruction data in the communication request registration area are cleared. (Always refer to (2) in this chapter.)



(2) Resend request signal (Yn+7)

If, for any reason, there is no communication completion response signal for data transmitted by the PRC instruction,

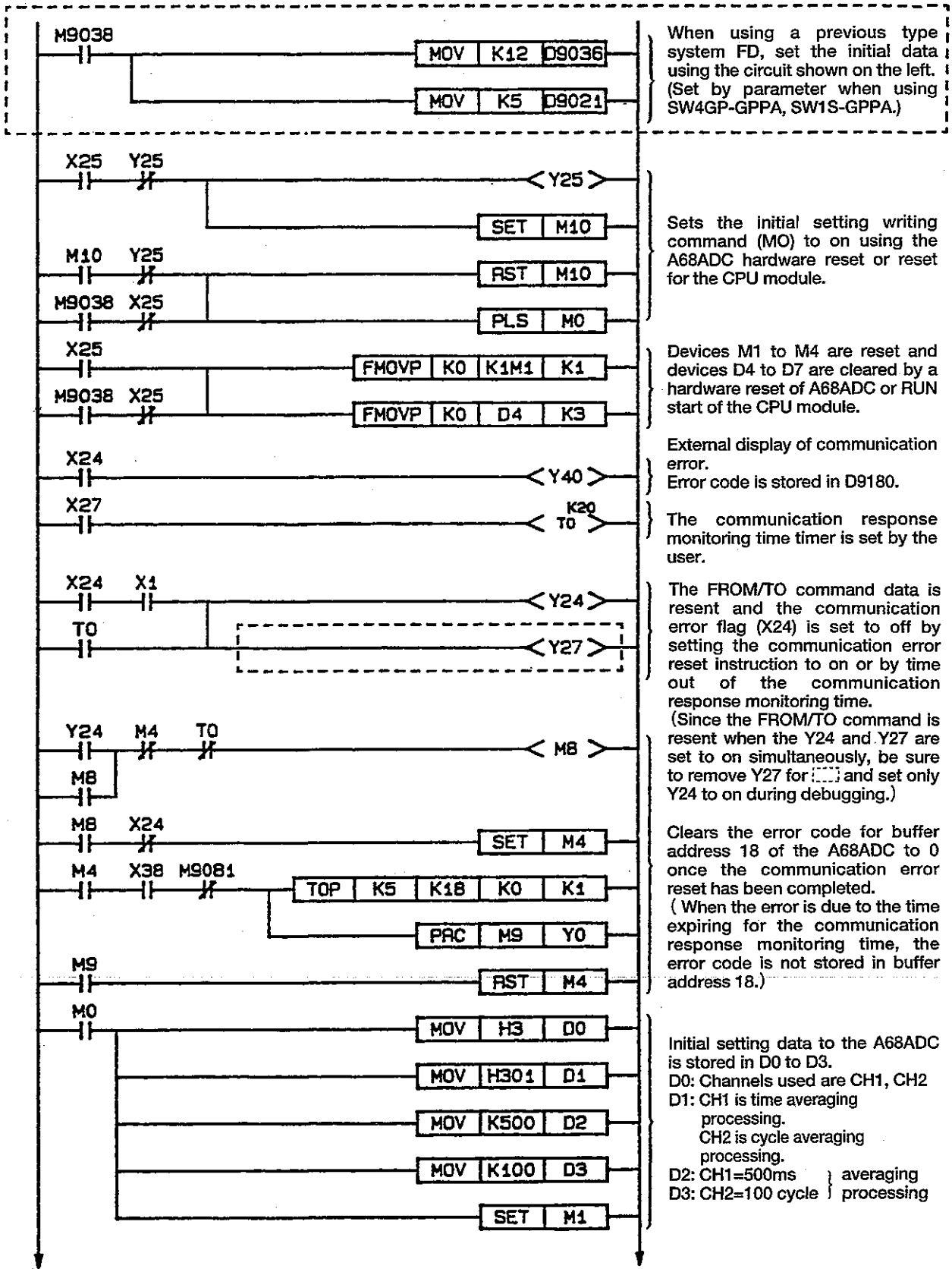
When data is transmitted again, the resend request signal (Yn+7) and communication error reset signal (Yn+4) are simultaneously set to on by the sequence program.



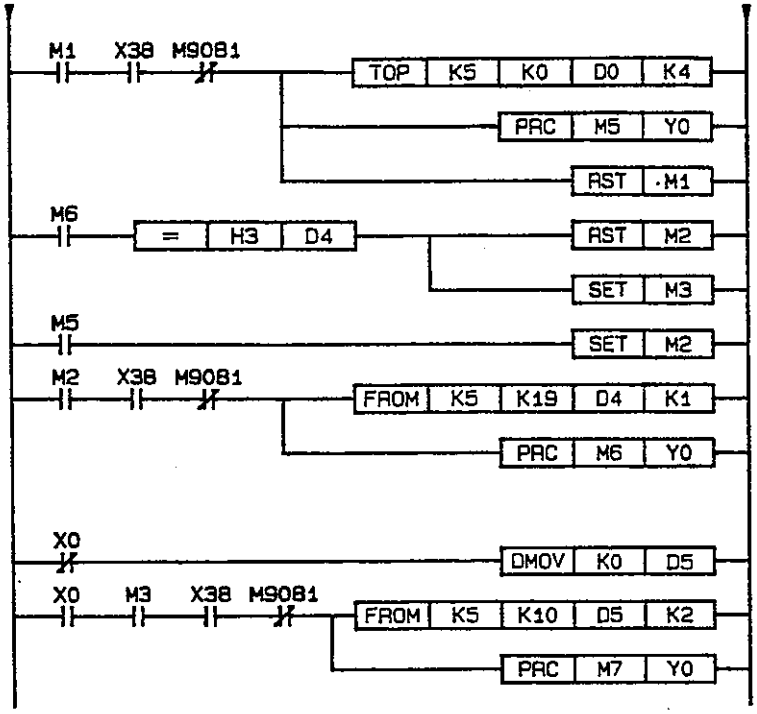
When the resend request signal (Yn+7) and communication error reset signal (Yn+4) are simultaneously set to on, the communication completion response signal wait flag (Xn+7) are temporarily set to off and previously executed FROM/TO instruction data stored in the communication request registration area is sent once again.

APP

Appendix 2 Program example when combining Version B of A68ADC and Version B of A2CCPU.



APP



The initial data stored in D0 to D3 is written to A68ADC buffer memory address 0 to 3.

After the initial setting data has been written to A68ADC, the A/D conversion completion flag is read from buffer memory address 19.
A/D conversion completion flag reading is stopped by A/D conversion completion at both CH1 and CH2 (3H) and setting digital output value reading permissive to on (M3).

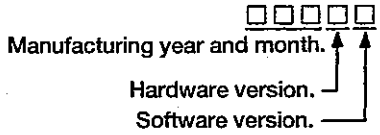
Digital output values for CH1 and CH2 are read to D5 and D8 when digital output read instruction (X0) is set to on.

Appendix 3 How to read the software version of each module

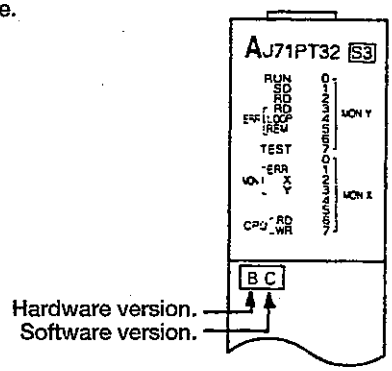
The method for determining the software version for each module A68ADC, A2CCPU, AJ71PT32-S3 is shown below.

(For A68ADC、A2CCPU)

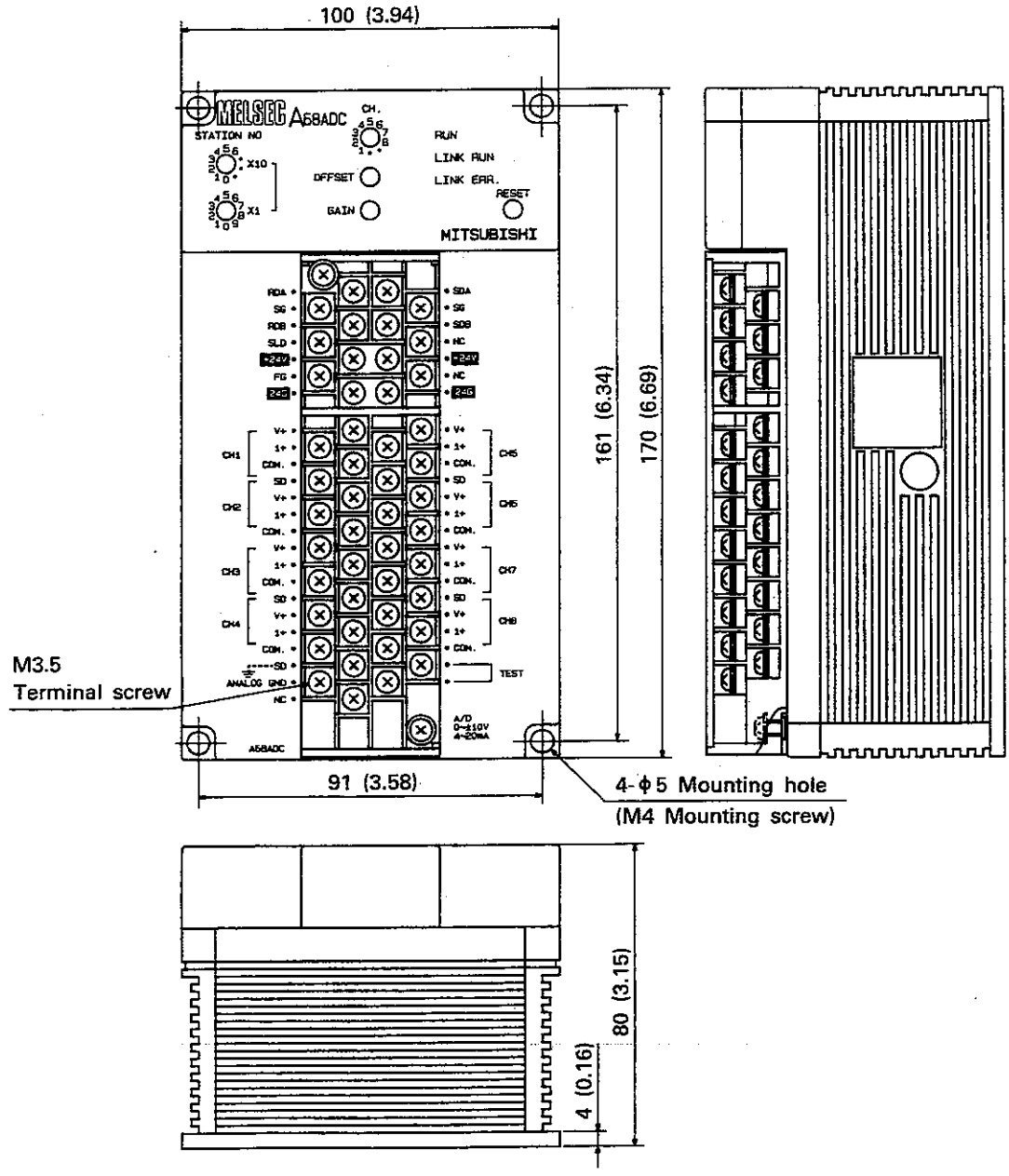
Date column on each plate.



(For AJ71PT32-S3)

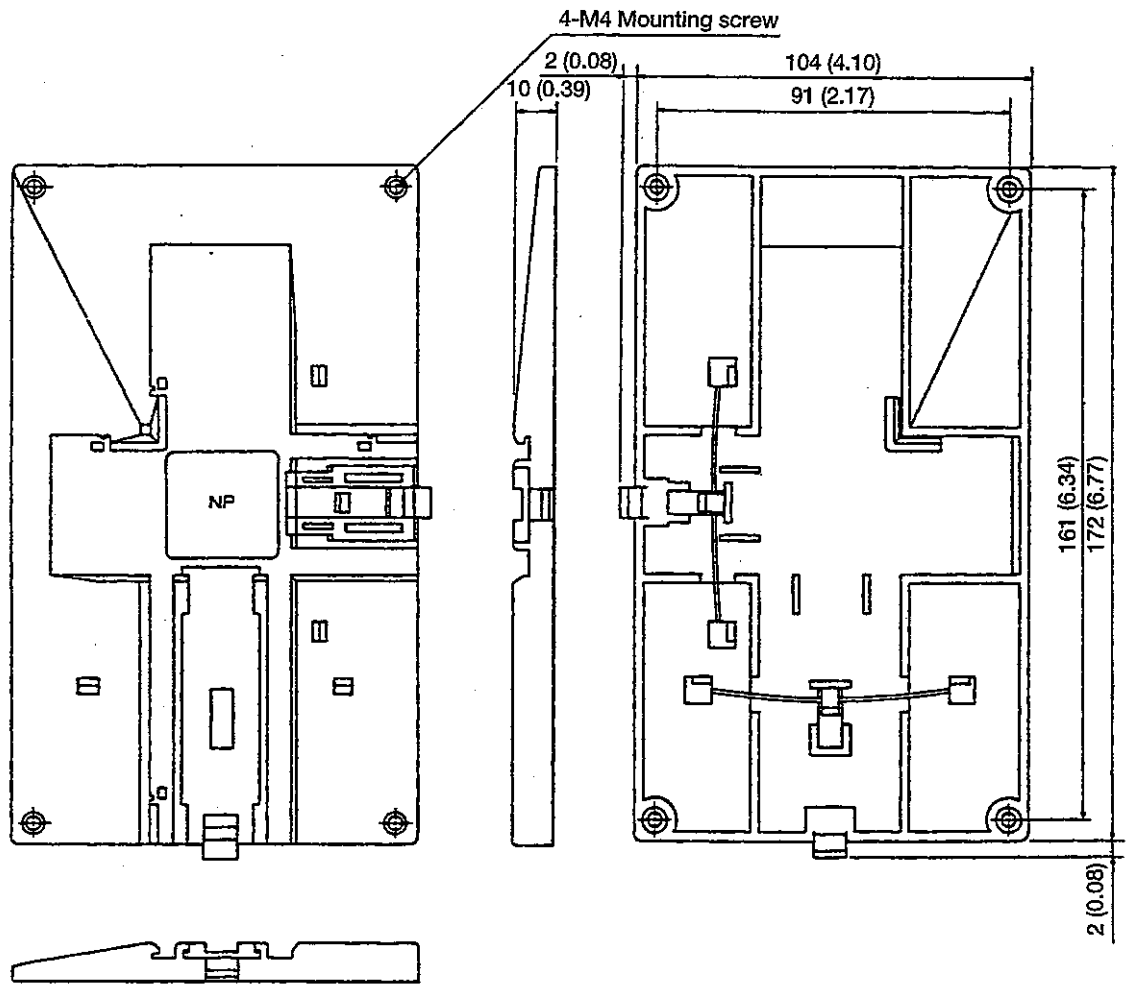


Appendix 4 Outside Dimensions



Unit: mm (in)

Appendix 5 DIN Rail Adapter Outside Dimensions



Unit: mm (in)

MEMO

WARRANTY

Please confirm the following product warranty details before starting use.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cast via the dealer or Mitsubishi Service Company. Note that if repairs are required at a site overseas, on a detached island or remote place, expenses to dispatch an engineer shall be charged for.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place.

Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautiors, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found to not be the responsibility of Mitsubishi or the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not possible after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of chance loss and secondary loss from warranty liability

Regardless of the gratis warranty term, Mitsubishi shall not be liable for compensation to damages caused by any cause found not to be the responsibility of Mitsubishi, chance losses, lost profits incurred to the user by failures in Mitsubishi products, damages and secondary damages caused from special reasons regardless of Mitsubishi's expectations, compensation for accidents, and compensation for damages to products other than Mitsubishi products and other duties.

5. Changes in product specifications

The specifications given in the catalogs, manuals or technical documents are subject to chage without prior notice.

6. Product application

(1) In using the Mitsubishi MELSEC programmable logic controller, the usage conditions shall be that the application will not lead to a major accident even if any problem or fault should occur in the programmable logic controller device, and that backup and fail-safe functions are systematically provided outside of the device for any problem or fault.

(2) The Mitsubishi general-purpose programmable logic controller has been designed and manufactured for applications in general industries, etc. Thus, applications in which the public could be affected such as in nuclear power plants and other power plants operated by respective power companies, and applications in which a special quality assurance system is required, such as for each Japan Railways company or the Department of Defense shall be excluded from the programmable logic controller applications.

Note that even with these applications, if the user approves that the application is to be limited and a special quality is not required, application shall be possible.

When considering use in aircraft, medical applications, railways, incineration and fuel devices, manned transport devices, equipment for recreation and amusement, and safety devices, in which human life or assets could be greatly affected and for which a particularly high reliability is required fin terms of safety and control system, please consult with Mitsubishi and discuss the required specifications.

Analog-Digital Converter Module type A68ADC

User's Manual

MODEL	A68ADC-USERS-E
MODEL CODE	13J782
IB(NA)-66247-B(0104)MEE	

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : 1-8-12, OFFICE TOWER Z 14F HARUMI CHUO-KU 104-6212,JAPAN
NAGOYA WORKS : 1-14 , YADA-MINAMI 5 , HIGASHI-KU, NAGOYA , JAPAN